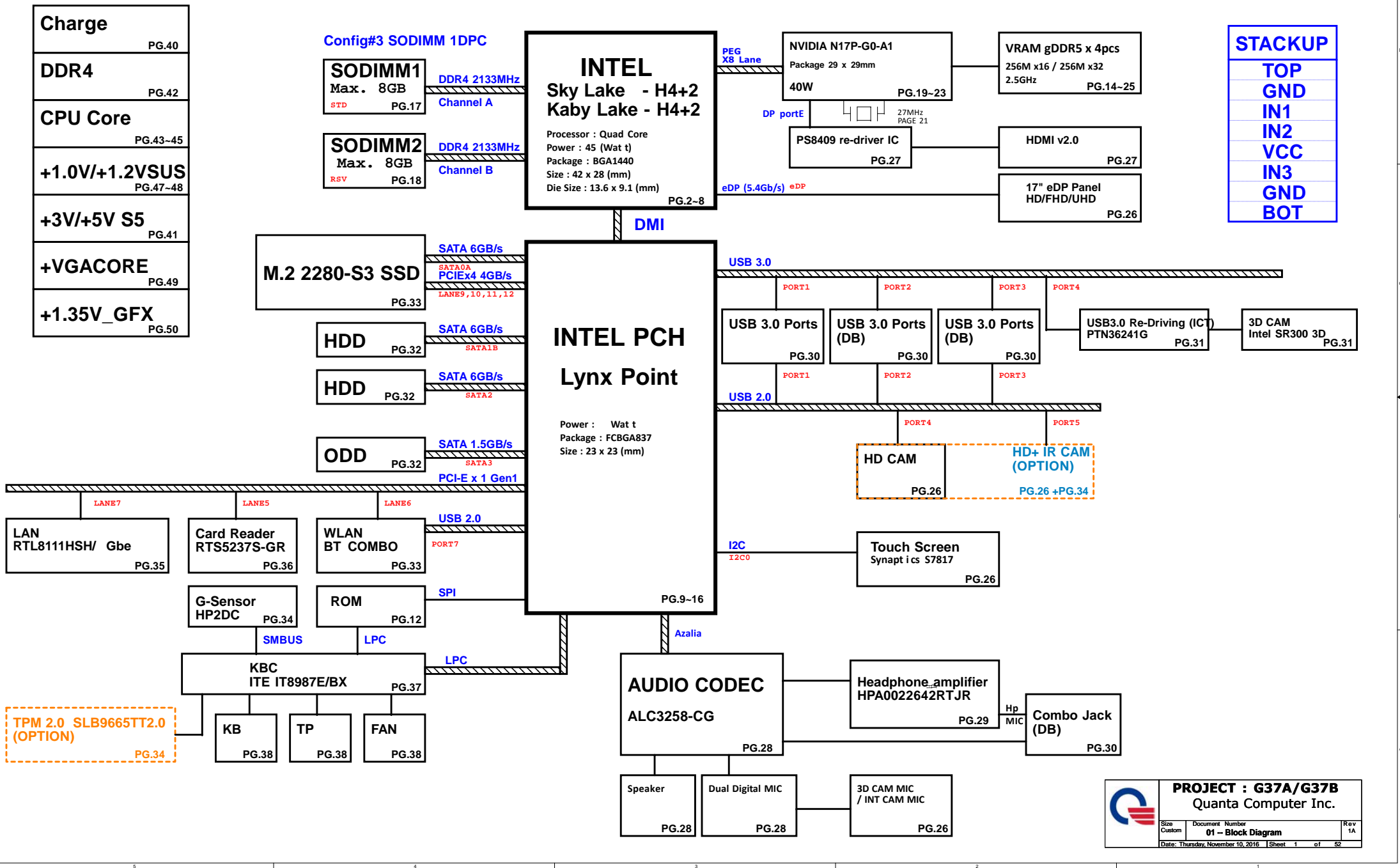
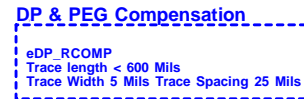
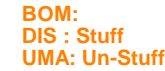
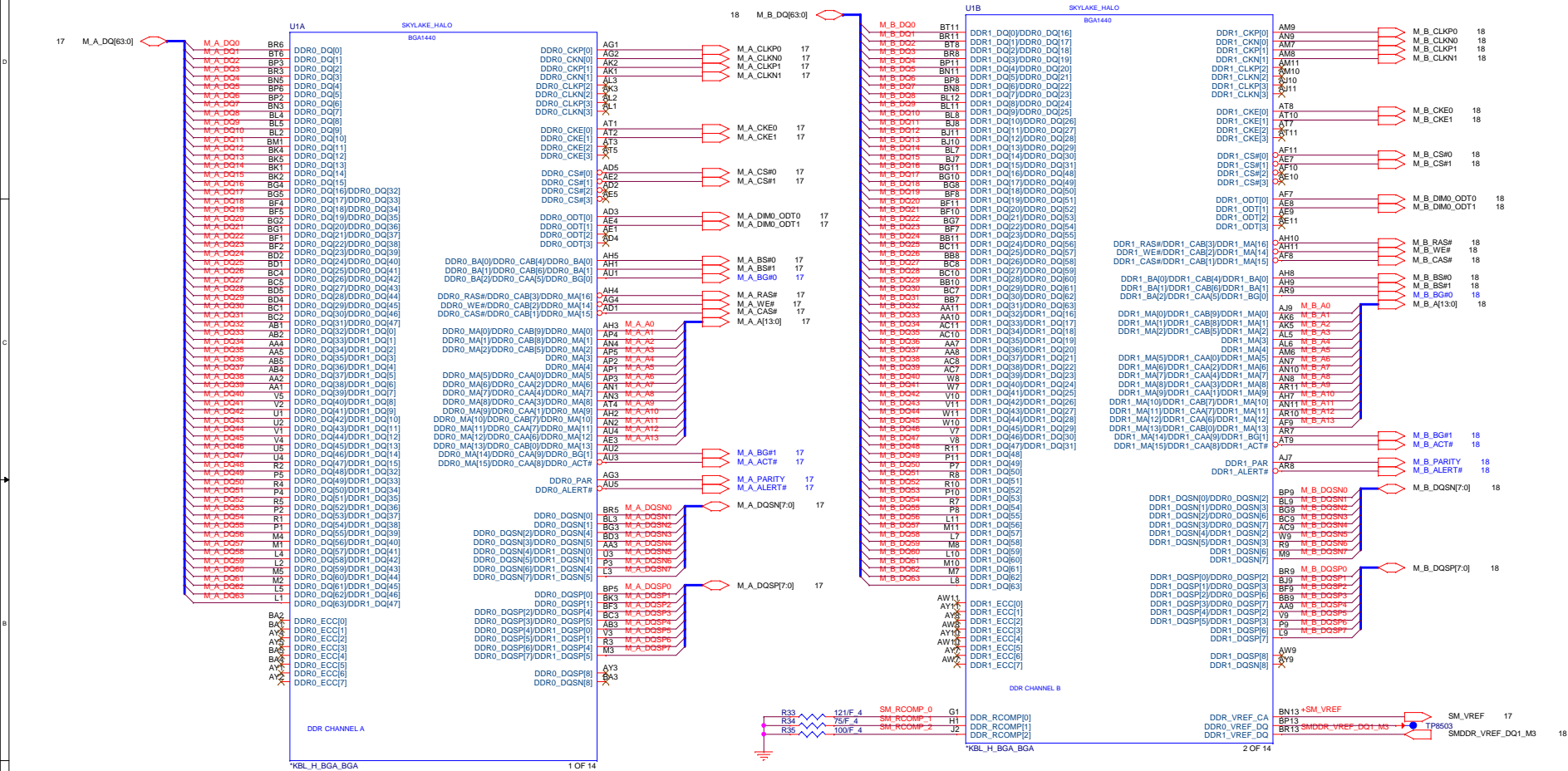


POWER PAVILION PARFAIT INTEL SKL / KABY -H SYSTEM DIAGRAM 01





Kaby Lake Processor (DDR4)



PROJECT : G37A/G37B
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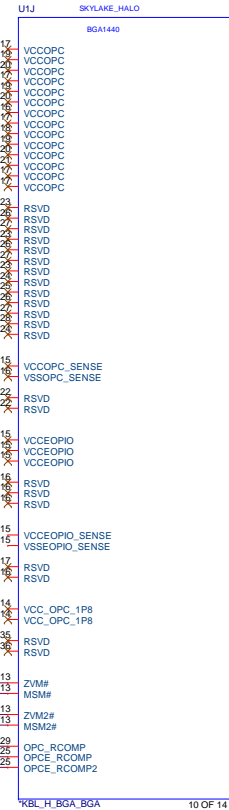
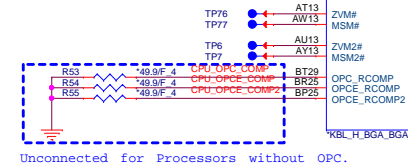
Size Custom	Document Number 04 -- SKL 3/7 (DDR4 I/F)	Rev 1A
Date: Thursday, November 10, 2016		Sheet 4 of 52

VCCGT_SENSE AH38 VCCGT_SENSE 4
VSSGTX_SENSE AH35
VSSGT_SENSE AH37 VSSGT_SENSE 43
VCCGTX_SENSE AH36

For 75 degree, 1.2v limit, (HW)

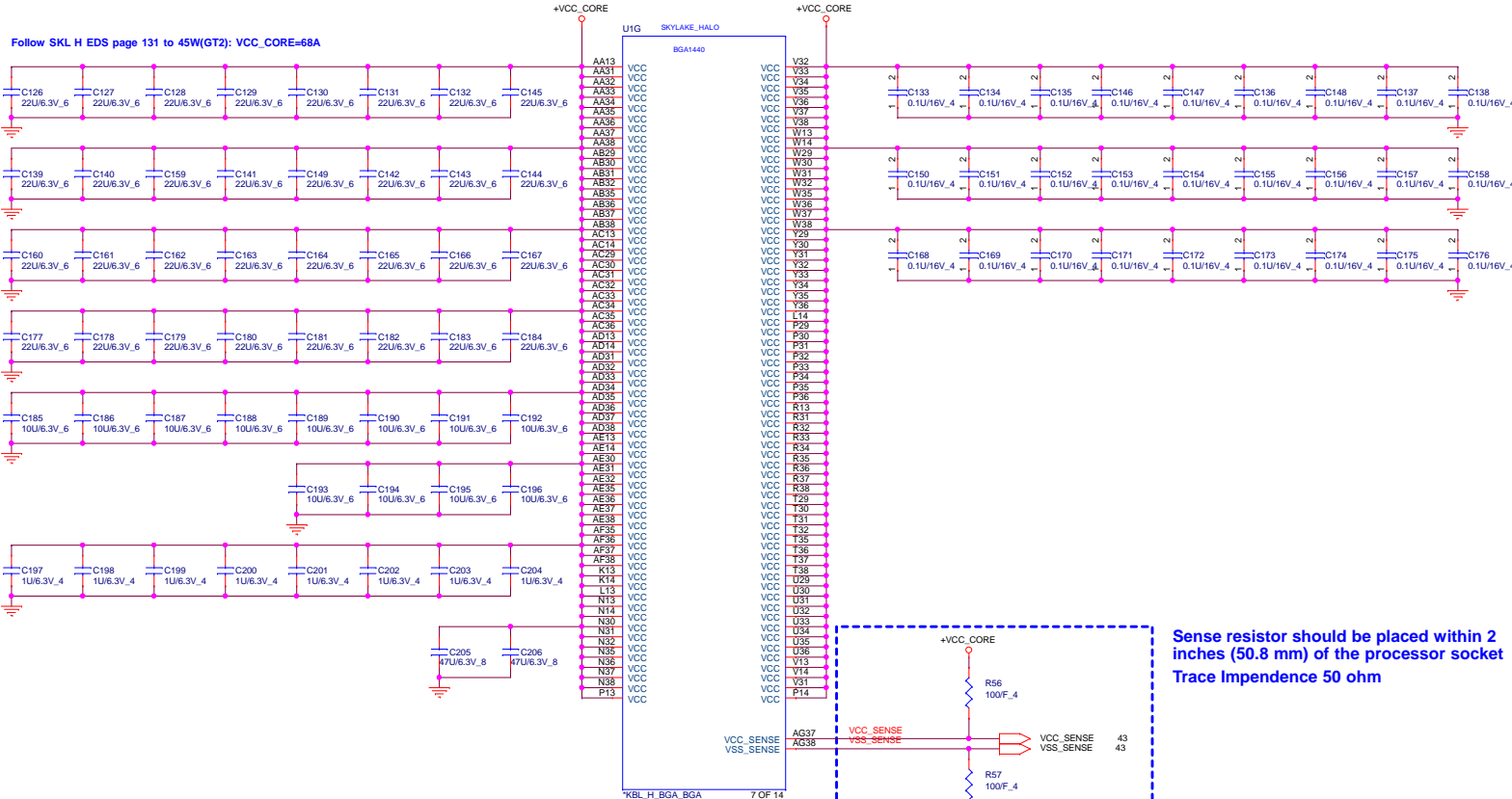
[illegible]

Follow SKL H EDS page 135 45W: VDDQ=2.8A

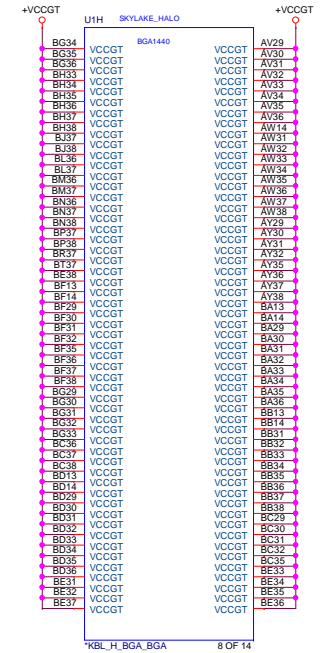


+VCC_CORE 44
+VCCGT 5,43,45

Follow SKL H EDS page 131 to 45W(GT2): VCC_CORE=68A



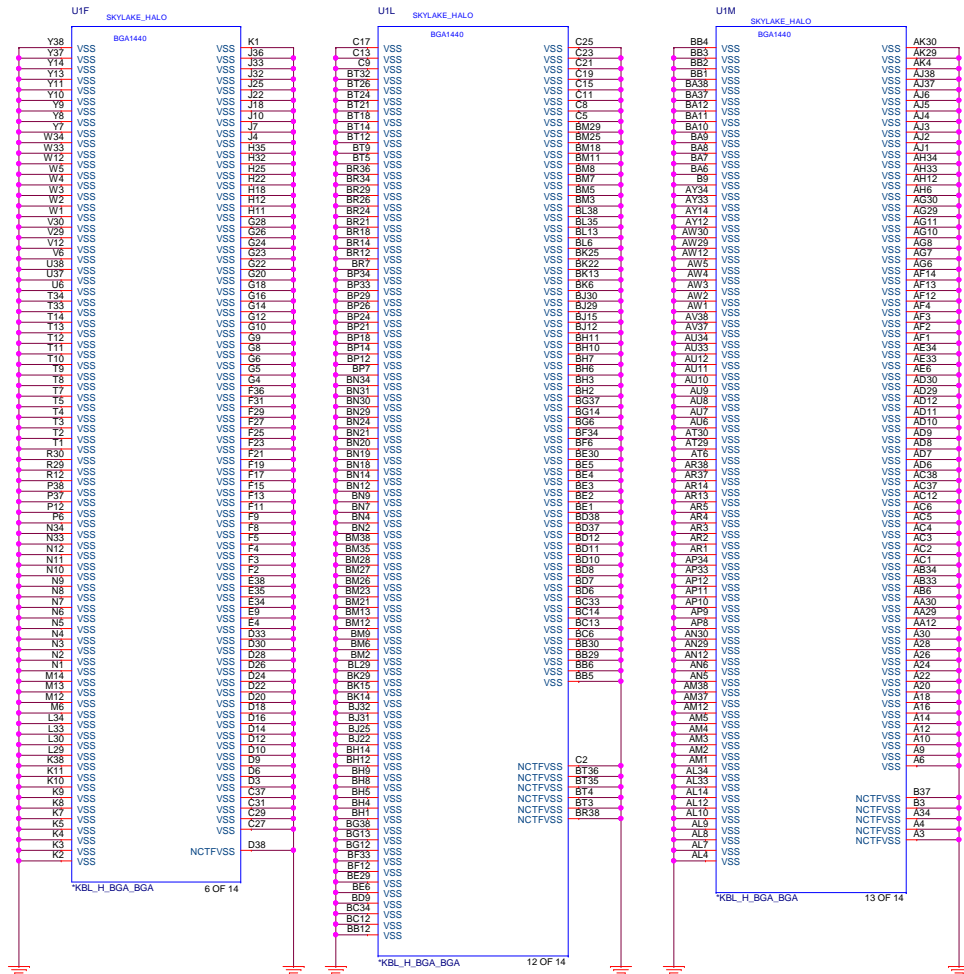
Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket
Trace Impedance 50 ohm



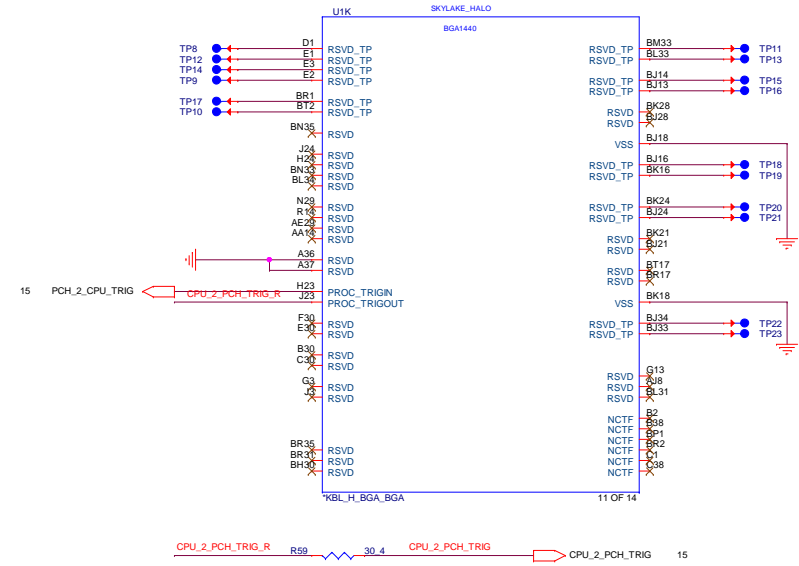
PROJECT : G37A/G37B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	07 - SKL 6/7 (POWER&GND)	1A
Date: Thursday, November 10, 2016 Sheet 7 of 52		

KBL-HProcessor (GND)



KBL-H Processor (RESERVED, CFG)

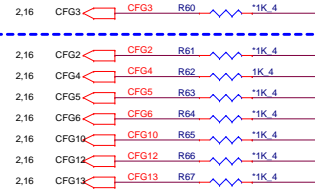


Processor Strapping

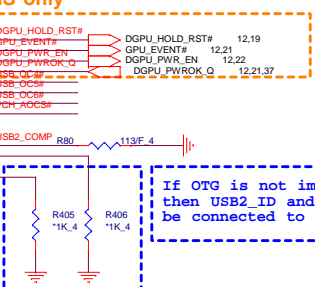
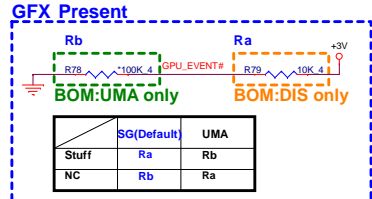
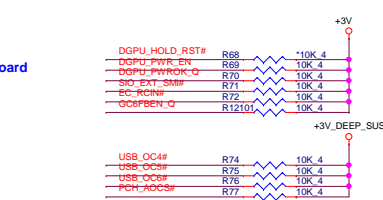
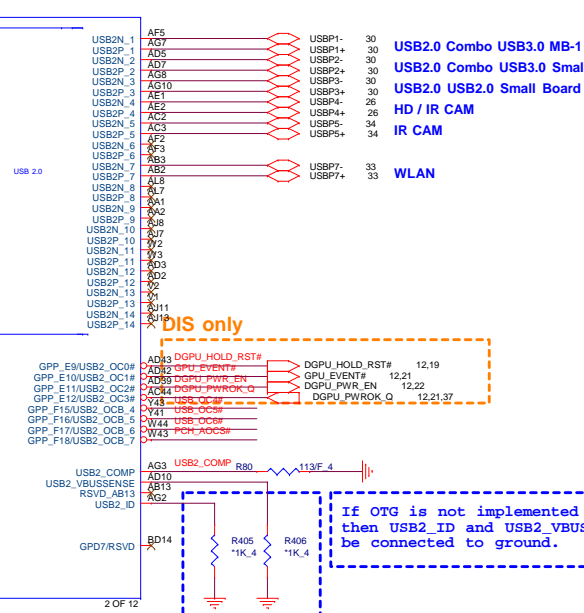
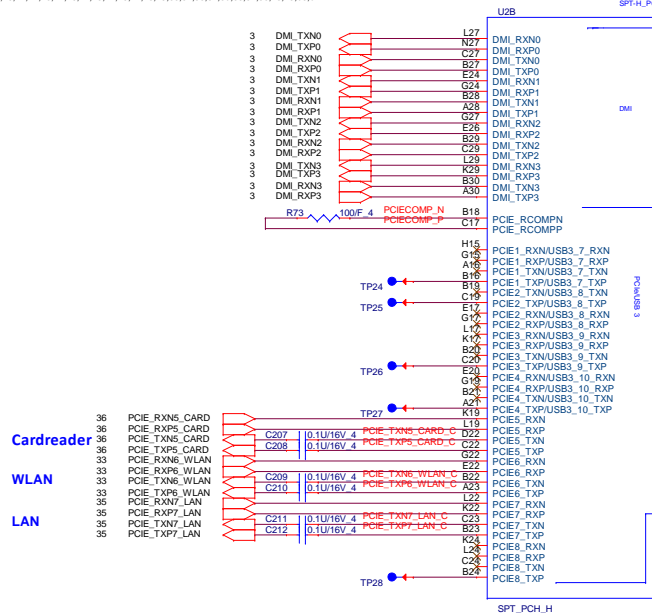
The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX ENABLED BIT IN DEBUG

1, Disable;



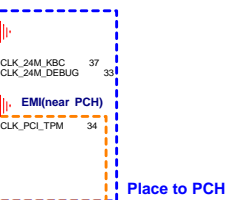
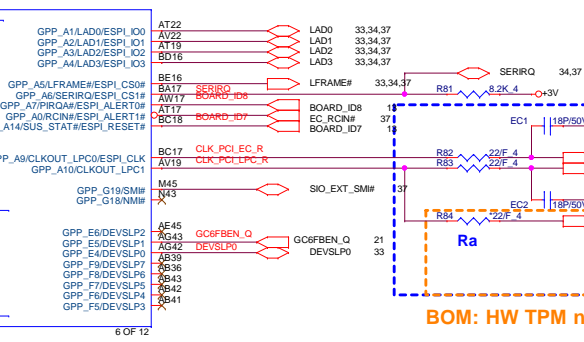
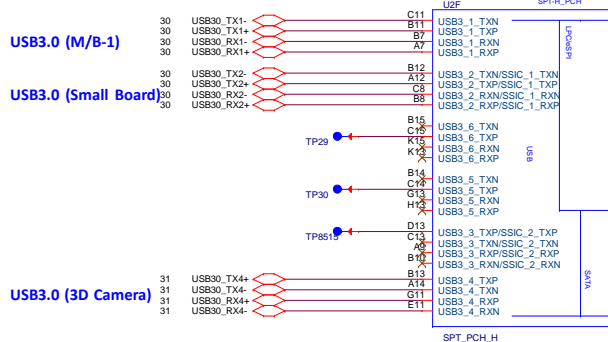
+3V DEEP_SUS 10,12,13,14,16,18
+3V 5,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51



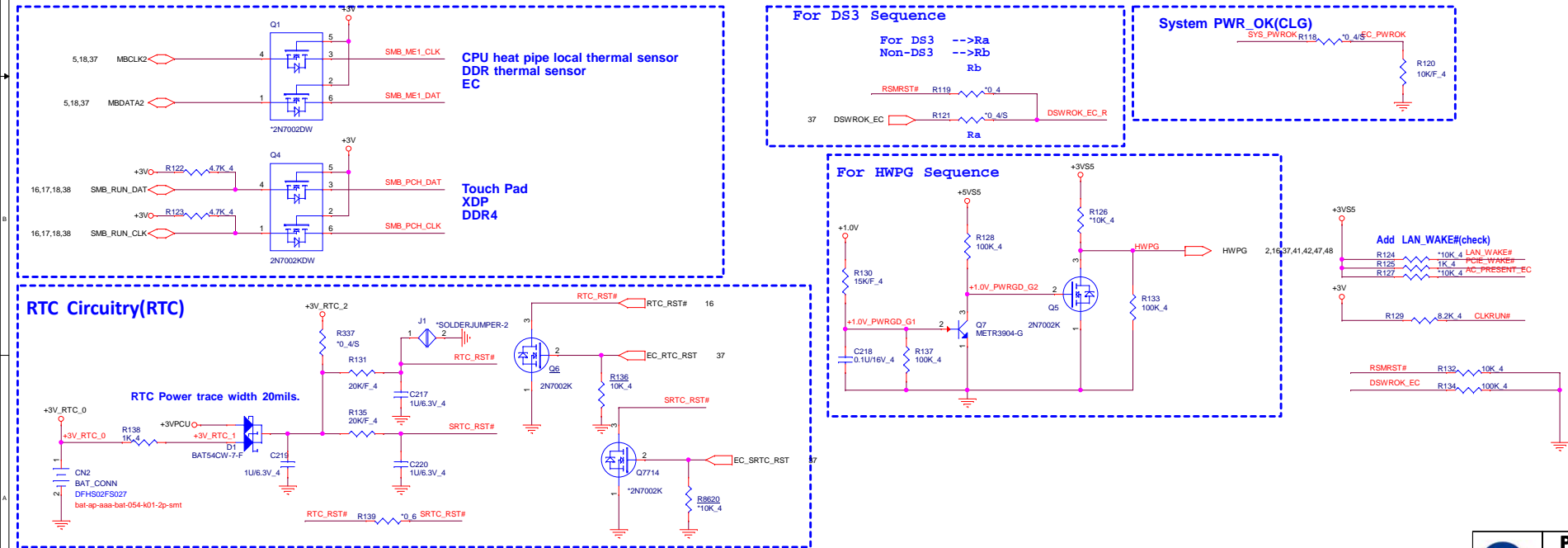
If OTG is not implemented on the platform, then USB2_ID and USB2_VBUSSENSE should both be connected to ground.

USB 2.0 PORT	
PORT1	USB2 MB
PORT2	USB2 DB
PORT3	USB2 DB
PORT4	HD /IR CAM (OPTION)
PORT5	IR CAM (OPTION)
PORT6	NC
PORT7	WLAN
PORT8	NC
PORT9-14	NC

USB 3.0 PORT	
PORT1	USB3 MB
PORT2	USB3 DB
PORT3	NC
PORT4	3D CAMERA



BOM: HW TPM need Ra, Rc Stuff



+3V 5.9,10,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51
+1.0V_DEEP_SUS 10,14,16,47,48

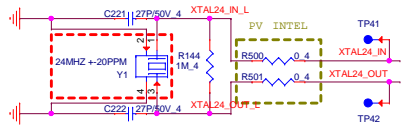
HSIO MUX PORT	
PCIE1-4	NC
PCIE5	Cardreader
PCIE6	Wlan
PCIE7	Lan
PCIE8	NC
PCIE9/SATA0A	
PCIE10	SSD PCIE x 4
PCIE11	
PCIE12	
PCIE13	NC
PCIE14	HDD-1
PCIE15	HDD-2
PCIE16	ODD
PCIE17	NC
PCIE18-20	NC

SSD PCIE x4 LANE

HDD-1 (SATA1B 6Gb/s)

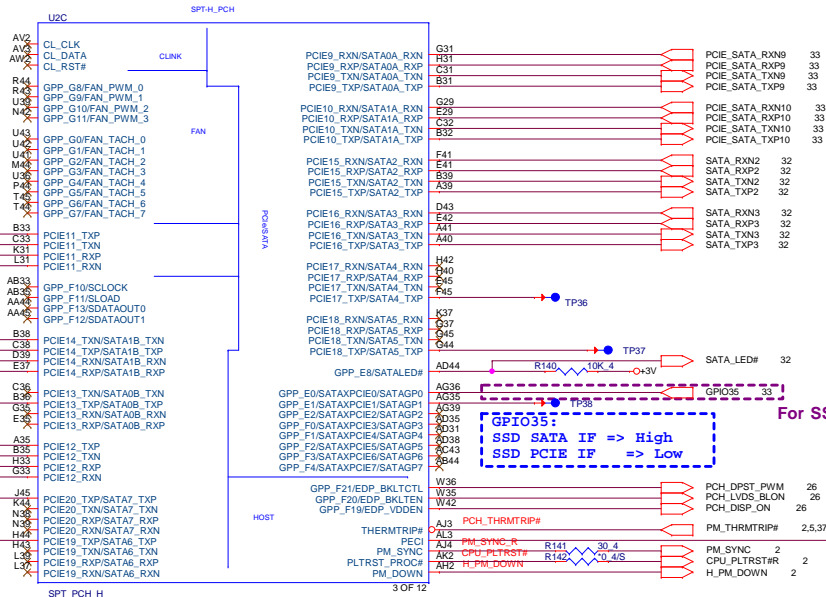
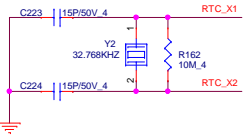
SSD PCIE x4 LANE

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.



Crystal Components with Surrounding 10 mil Wide GND Shield Trace Break Out: 4-10 mil Wide GND Shield Trace

RTC Clock 32.768KHz



SSD PCIE x4 (SATA0A) LANE

SSD PCIE x4 LANE

HDD-2 (SATA2 6Gb/s)

ODD (SATA3 3.0Gb/s)

For SSD Det (SATA0A)

BOM:SSD only

GPIO35:
SSD SATA IF => High
SSD PCIE IF => Low

PCH_PECI 2

PCH_PECI 2

PCH_PECI 2

PCH_PECI 2

PCH_PECI 2

PCH_PECI 2

PCH_PECI 2

PCH_PECI 2

PCH_PECI 2

PCH_PECI 2

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PCH_PECI 2

PCH_PECI 2

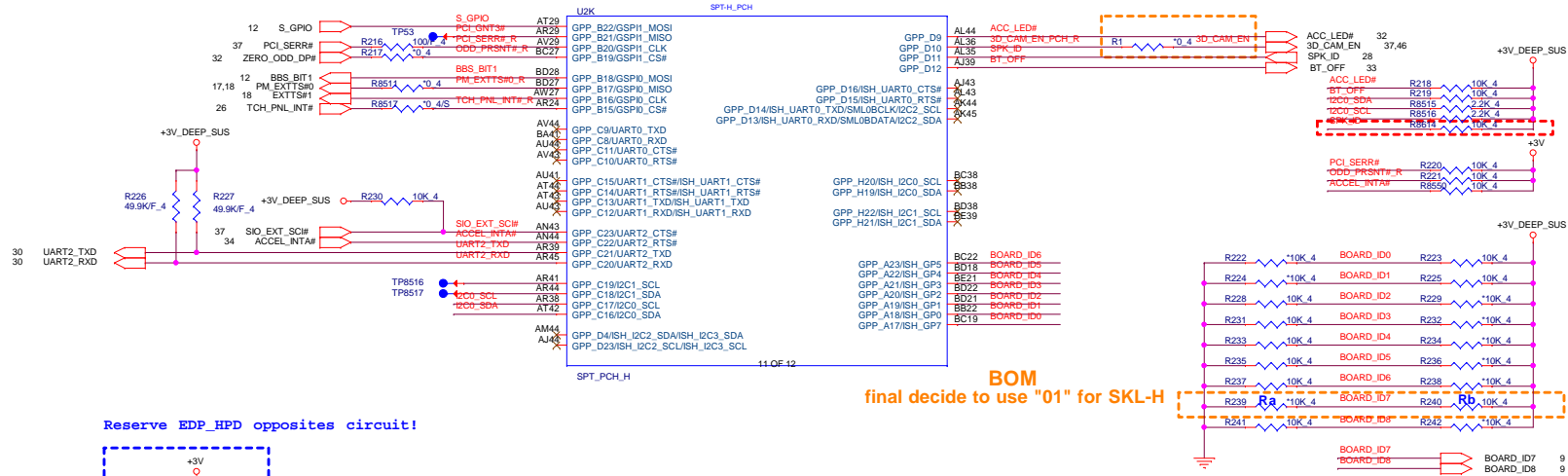
PCH_PECI 2



PROJECT : G37A/G37B
Quanta Computer Inc.

Size Custom Document Number 11 - PCH 3/7 (SATA/LPC/CLK) Rev 1A
Date: Thursday, November 10, 2016 Sheet 11 of 52

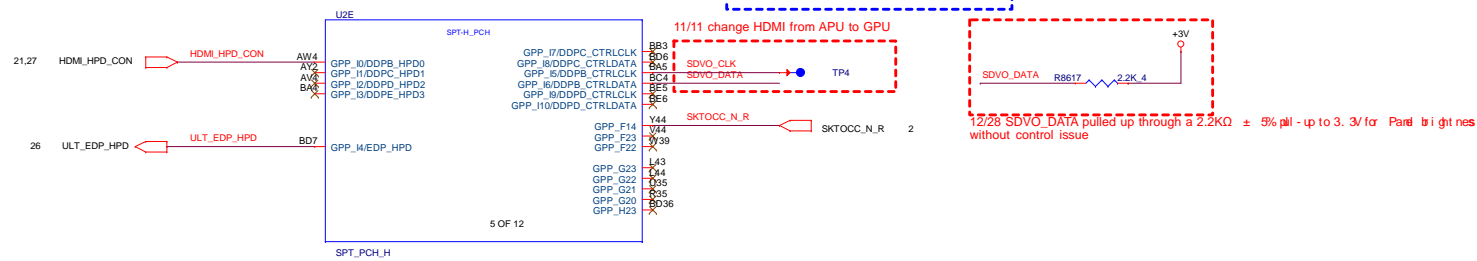
3D CAMERA BOM: 3D CAM Un-Stuff (EN will from EC control)



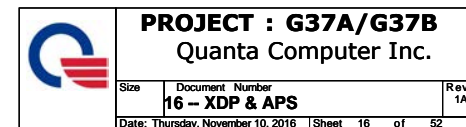
BOM final decide to use "01" for SKL-H

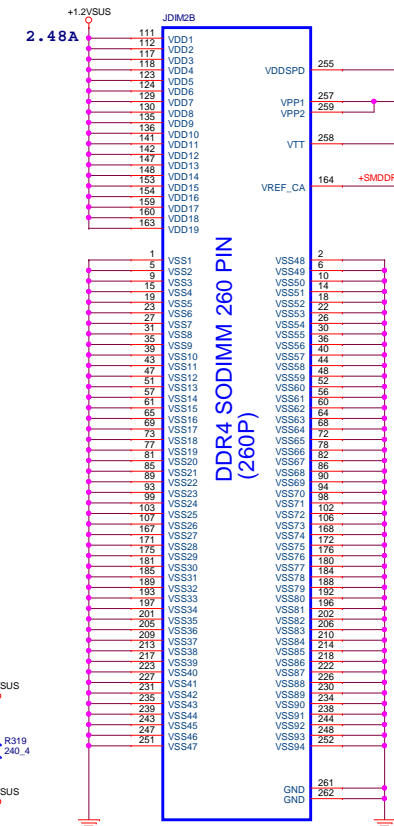
Model	BOARD_ID[8:7] ID8;ID7	BOARD_ID[6:5] ID6;ID5	Board ID [4:3] ID4;ID3	BOARD_ID[2:1] ID2;ID1	BOARD_ID0 ID0
Definition	00 Non 3D CAM 01 3D CAM	00 Reserved	Reserved	00 15" P SKL H 01 17" P SKL H 10 17" SP SKL H 11 17" KBL H	0 : U M A 1 : D S

This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.

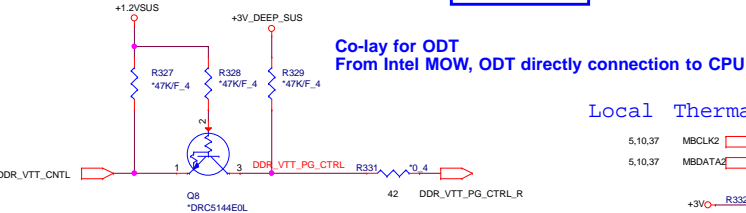








VREF DQ1 M1 Solution



UB

1 SCLK VCC

2 SDA DXP

3 ALERT# DYN

4 OVERT# GND

5

1 C327 *0.01u50V 4

2 DDR_THERMDA

3 C328 *220p/50V 4

4 DDR_THERMDC

5

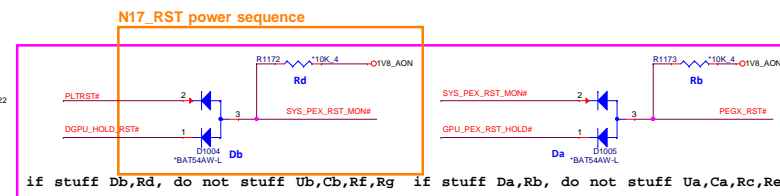
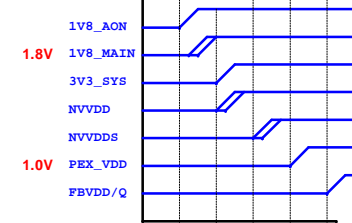
Q9 METR3904-G

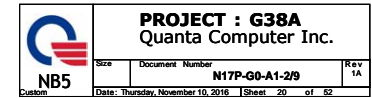
DDR4 Thermal Sensor

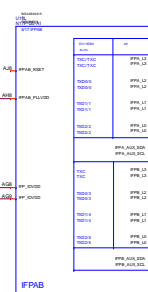
*TMP431ADGKR
I2C4 Check PR1 (SD)

Main:AL001412003
2nd:AL000431014

EMC14C12-1ACZL-TR(98h)
TMP431ADGKR(98h)







STRAP[2:0] VRAM Table for N17P-G0 GDDR5 Recommended Memories

STRAP[2:0]	DESCRIPTION	Vendor	Vendor PN	TOP P/N	OS P/N	Default
S0	GDDR5 256Mx32 7 Gns	SamSung B die	K4D513238E-1028	AKGSG00D150	AKGSG00D150	
S1	GDDR5 256Mx32 7 Gns	Metrix A die	M51212583382-701A	AKGSG00D157	AKGSG00D150	
S2	GDDR5 256Mx32 7 Gns	Hynix A die	H5GQ8324A78-B0C			
S3	GDDR5 128Mx32 7 Gns	SamSung E die	K4D413238E-1028	AKGSG00D151	AKGSG00D152	
S4	GDDR5 128Mx32 7 Gns	Metrix A die	K2M413238B3-70-P-JR	AKGSG00D158	AKGSG00D157	
S5	GDDR5 128Mx32 7 Gns	Hynix A die	H5GQ4824A78-B0C	AKGSG00D156	AKGSG00D153	

Vendor	Size	PN
NTE-DX	WBG000	8MB
NTE-DY	Giga device	1Mb

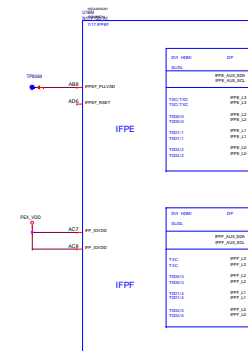
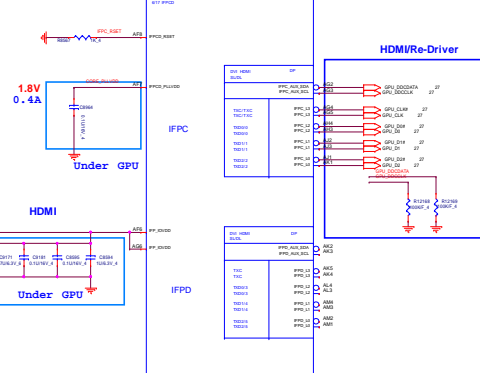


Table 14.2 GPIO Descriptions for GB4C-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	HWPGD_PWD_VID	O	Pin0 Output to control HWPGD	0 to VDD Pin output
GPIO1	GCMAI_GCK_P8_DI	O	FB Enable for GCK 2.1	Open Source 10 kΩ pull-down
GPIO2	GCMAI_GPU_RESET	I	GPU reset signal for GCK 2.1	100 kΩ pull-up to VDD_ACH, unless driven actively
GPIO3	HWPGD_STAN_PWD	O	Pin0 output to control the STAN power supply	0 to VDD output
GPIO4	GCMAI_HL_NAR_PWD	O	GPU power sequencing for GCK 2.1	Open Drain 100 kΩ pull-up to VDD_ACH
GPIO5	FWM_LCK	I	Active low Frame Lock	Open Drain 100 kΩ pull-up to VDD_ACH

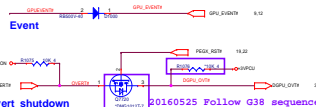
Table 14.3 GPIO Descriptions for GB4C-128 Packages (Continued)

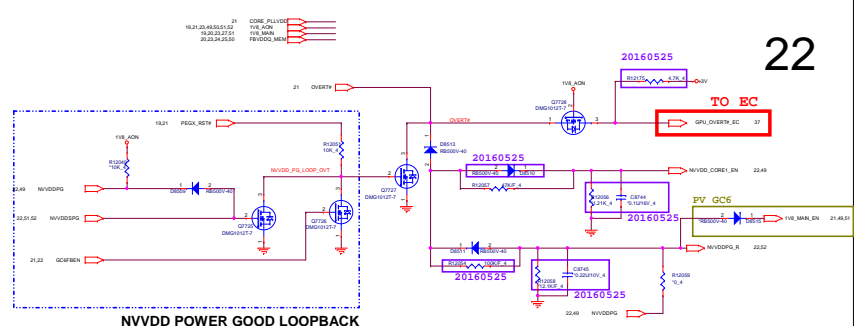
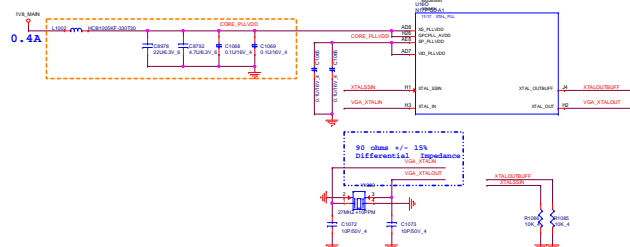
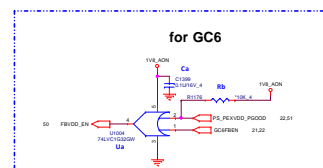
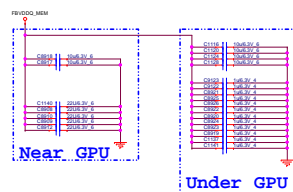
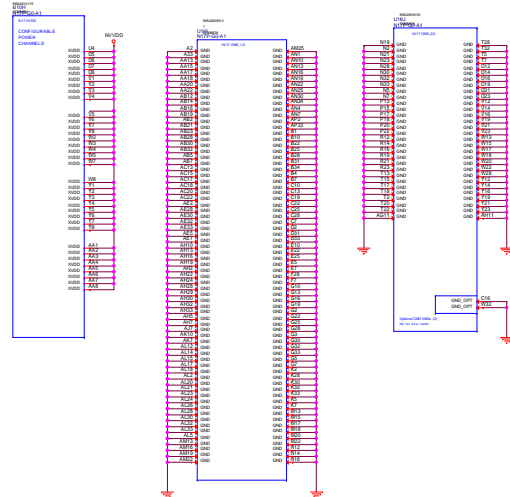
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO6	HWPGD_PSI	O	Phase Shedding (see Section 14.3.3)	10 kΩ pull-up to VDD_ACH to enable multiple phases
GPIO7	LED_BL_PWDN	O	Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pin up/pull-up to VDD to set the VDDA02 power mode
GPIO9	THRM_ALERT	I/O	Active Low Thermal Alert	Open Drain 100 kΩ pull-up to VDD_ACH
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LED_VDD	O	Quadro Power enable	100 kΩ pull-down
GPIO12	FWM_LEVEL	I	Power supply (FWM) input	100 kΩ pull-up to VDD_ACH
GPIO13	LED_BLEN	O	LED Backlight Enable	Panel Backlight Enable
GPIO14	HPD_PPFA	I	Hot Plug Detect for HPFA	Inverted input. See Figure 14.3
GPIO15	HPD_PPFD	I	Hot Plug Detect for HPFD	Inverted input. See Figure 14.3
GPIO16	GCMAI_PCH_RST_ACH	O	System side PCIe reset monitor	10 kΩ pull-up to VDD_ACH unless actively driven
GPIO17	HPD_PPFD	I	Hot Plug Detect for HPFD	Inverted input. See Figure 14.3
GPIO18	HPD_PPFD	I	Hot Plug Detect for HPFD	Inverted input. See Figure 14.3
GPIO19	SD_VIDEN	O	SD Video I/O Signal	100 kΩ pull-down
GPIO20	FWM_MODE	I/O		
GPIO21	FWM_MODE	I/O		
GPIO22	FWM_MODE	I/O		

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO23	GCMAI_GPU_RESET_HOLDN	O	GPU PCIe self-reset control	Open Drain 10 kΩ pull-up to VDD_ACH
GPIO24	HPD_PPFD	I	Hot plug detect for HPFD	Inverted input. See Figure 14.3
GPIO25	UNUSED	O		
GPIO26	UNUSED	O		
GPIO27	HPD_PPFD	I	Hot plug detect for HPFD	Inverted input. See Figure 14.3

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO28	GPIO28	I/O	Catastrophic Over Temperature	100 kΩ pull-up to VDD_ACH

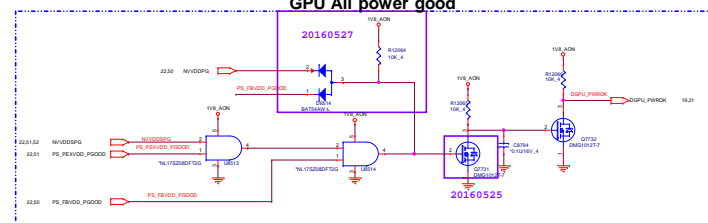




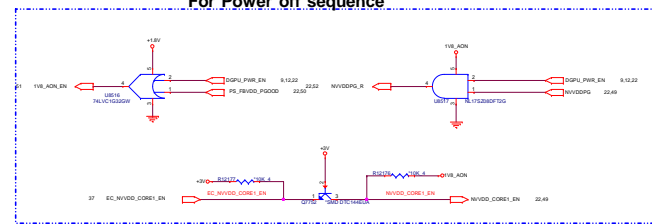
NVVDD POWER GOOD LOOPBACK

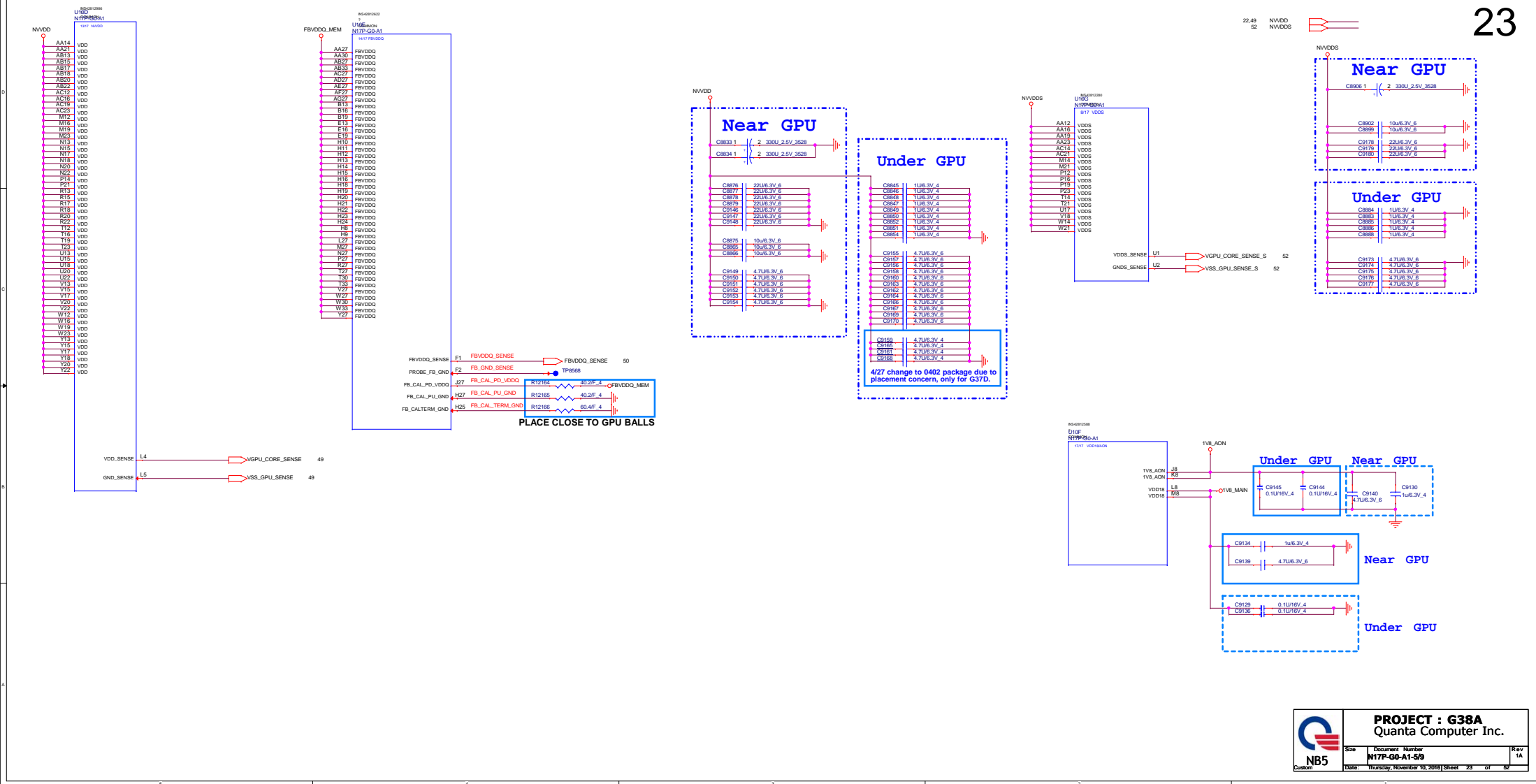
Overt temp ckt for NVVDD and NVVDDP

GPU All power good



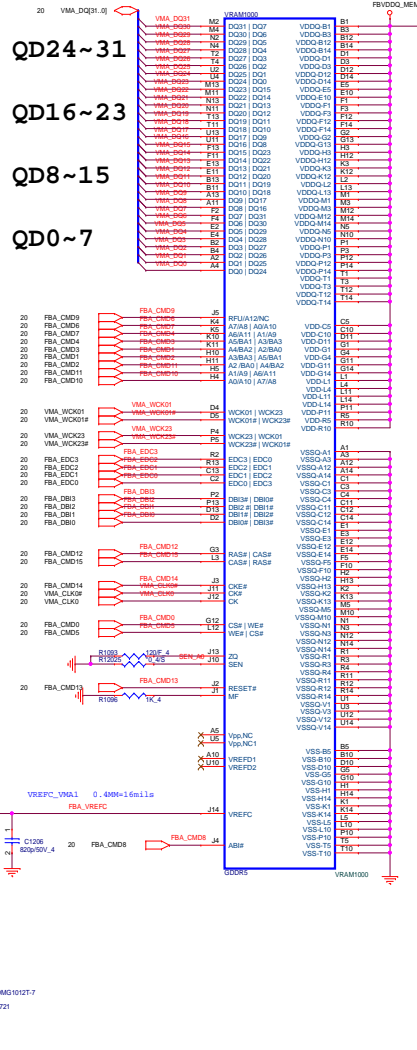
For Power off sequence





Channel 0
<0-31>

MF=0 Non-mirrored

Channel 1
<32-63>

MF=1 mirrored

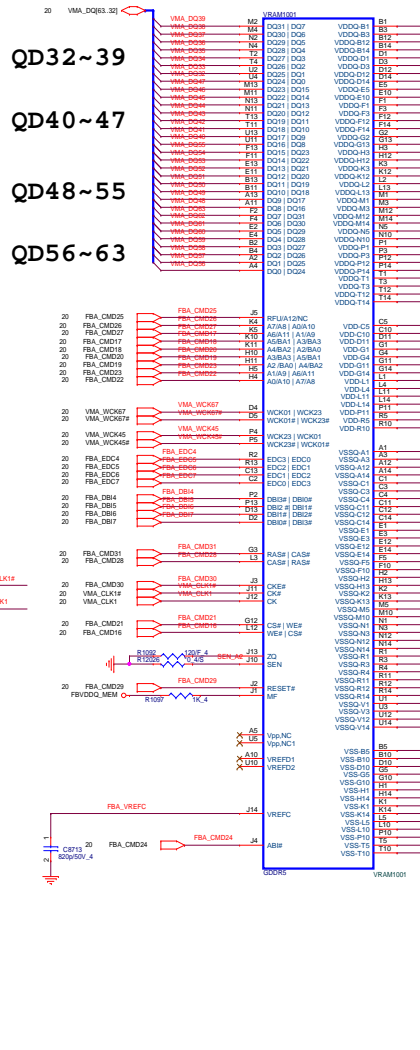


Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

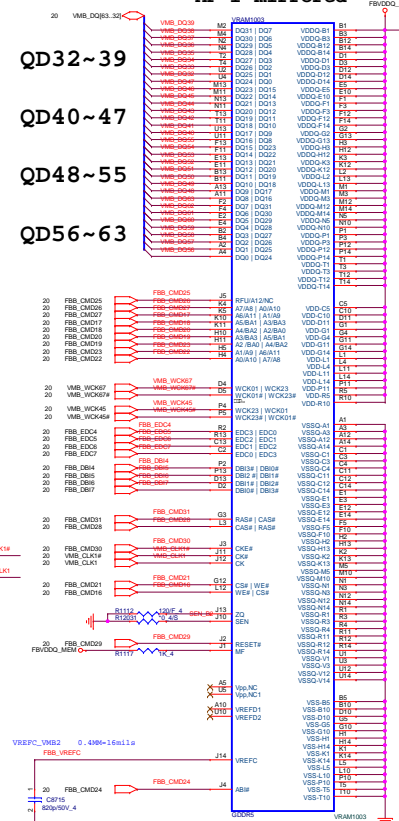
Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	AB*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	R1_R9
FBA_CMD13	FBA_CMD29	R5*
FBA_CMD14	FBA_CMD30	CHE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

20,22,23,24,50 FBVDDQ_MEM

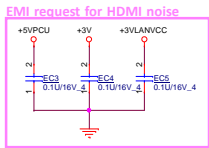
Channel 1
<32-63>
MF=1 mirrored



Command Ball on GPU	DRAM Signal Definition
---------------------	------------------------

Table 8.5 GDB55 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
---------------------	------------------------



GPU_D0 R8626 *120/F_4 GPU_D0#

GPU_D1 R8627 *120/F_4 GPU_D1#

GPU_D2 R8628 *120/F_4 GPU_D2#

GPU_CLK R8629 *120/F_4 GPU_CLK#

TX2_HDMI+	R7716	*120F_4	TX2_HDMI-
TX1_HDMI+	R7717	*120F_4	TX1_HDMI-
TX0_HDMI+	R7719	*120F_4	TX0_HDMI-
TXC_HDMI+	R7722	*120F_4	TXC_HDMI-

U7701

1 TxC_HDMI- 10 TxC_HDMI+

2 TxC_HDMI+ 9 NC

3 Tx1_HDMI- 8 NC

4 Tx1_HDMI+ 7 Tx1_HDMI-

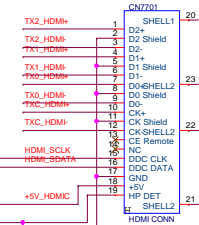
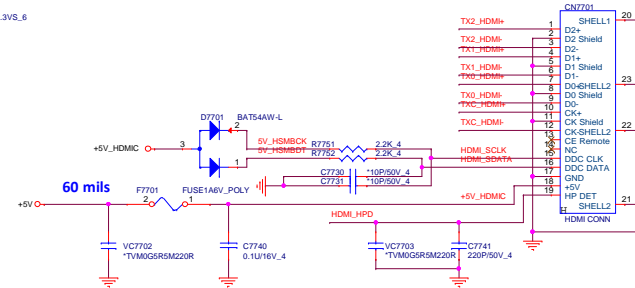
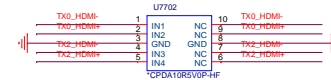
5 GND 6 Tx1_HDMI+

IN4 NC

IN3 GND

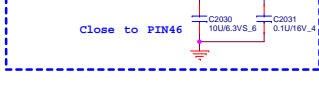
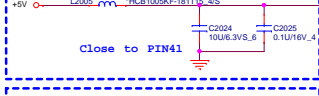
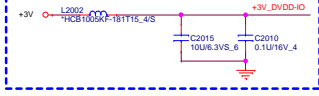
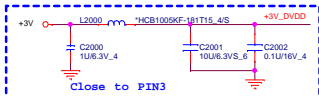
GND

CPDA10R5V0P-HF

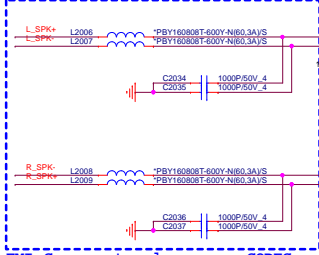


Size Custom	Document Number 27 -- HDMI/HDMI REDRIVER	Re 1
Date: Thursday, November 10, 2016	Sheet 27 of 52	

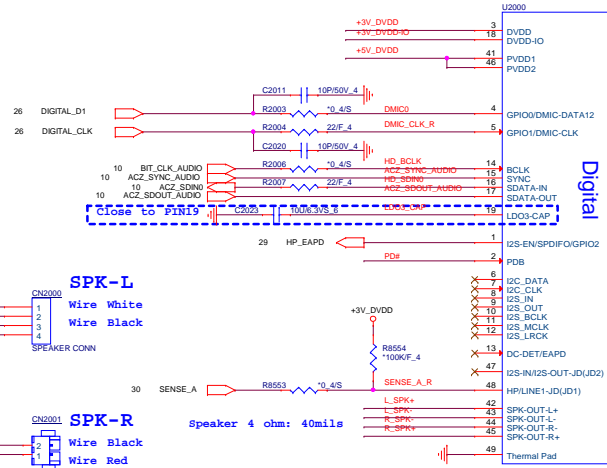
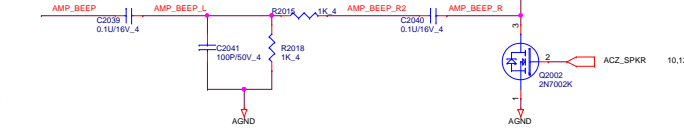
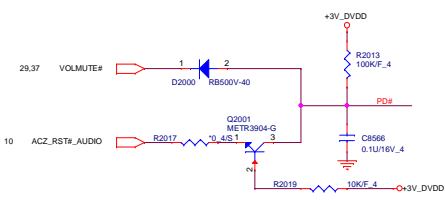
+5V 26,27,29,32,38,46,49
 +3V 5,9,10,11,12,13,14,16,17,18,22,26,27,29,30,32,33,34,35,36,37,38,43,46,50,51
 +1.8V 22,31,47,51



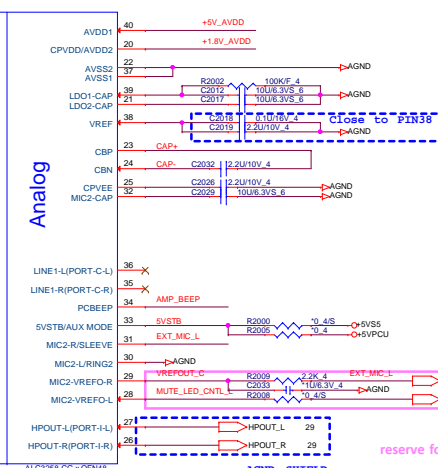
Speaker 4 ohm: 40mils



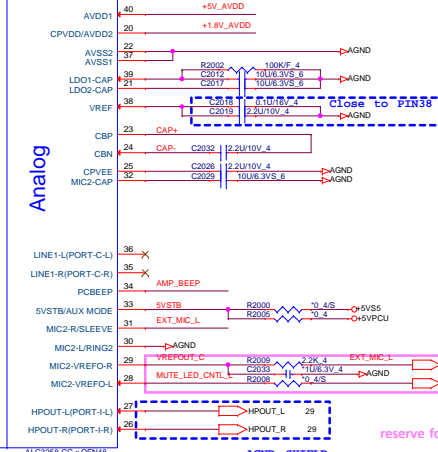
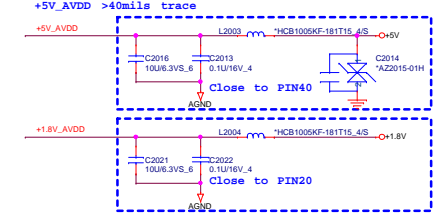
EMI Components place near CODEC



Digital

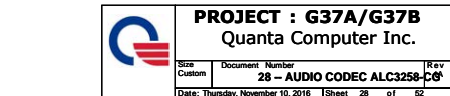


Analog



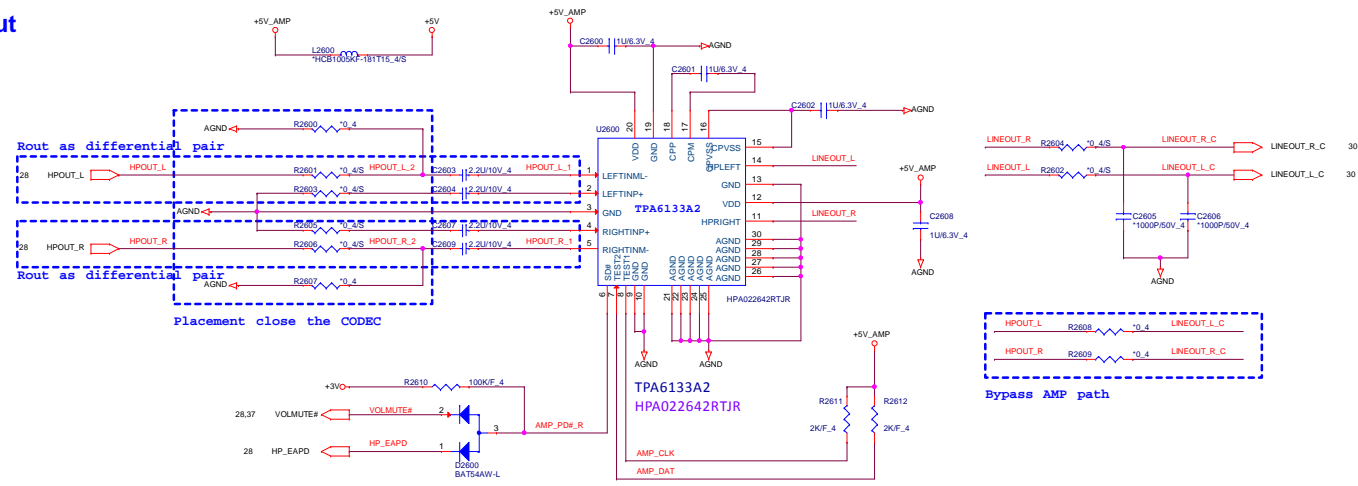
ALC3258-CG x QFN48


place to near or under codec



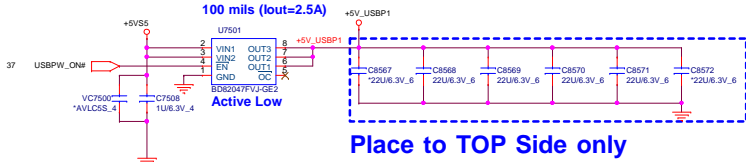
PROJECT : G37A/G37B		Rev
Quanta Computer Inc.		
Size	Document Number	
Custom	28 - AUDIO CODEC ALC3258-CG	Rev
Date: Thursday, November 10, 2016	Sheet 28 of 52	

Head Phone out



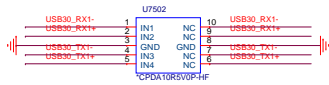
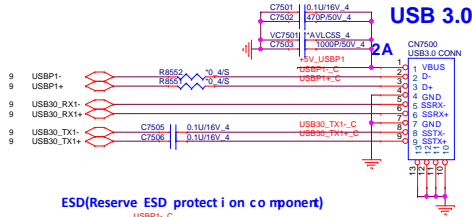
 PROJECT : G37A/G37B Quanta Computer Inc.		
Size	Document Number	Rev
Custom	29- HP AMP HPA022642RTJR	1A
Date: Thursday, November 10, 2016 Sheet 29 of 52		

+5VSS	10,28,41,42,43,44,45,46,47,48,49,50,51,52
+5VPCU	5,10,21,33,37,38,40,41
+3V	5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,32,33,34,35,36,37,38,43,46,50,51
+1.8V	22,28,31,47,51



USB 2.0/3.0 Combo

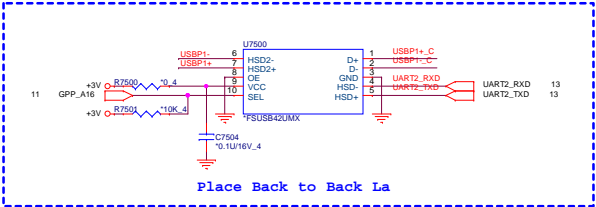
30



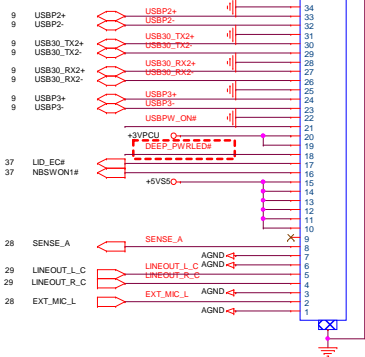
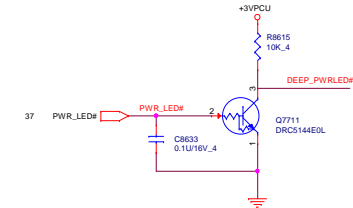
Daughter Board


51619-03401-001
51619-03401-001-34p-I
DFPC34FR030
CN7702

UART for Win7 WHQL DEBUG



PWR LED MOS Circuit





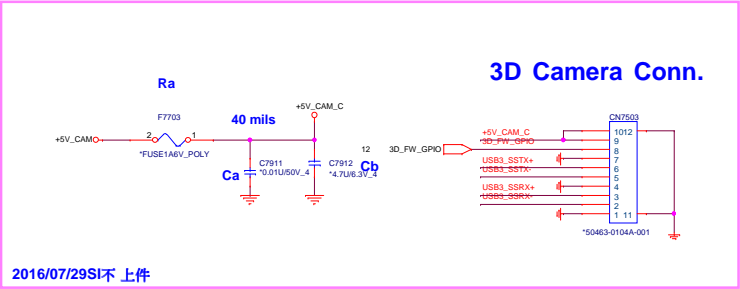
PROJECT : G37A/G37B

Quanta Computer Inc.

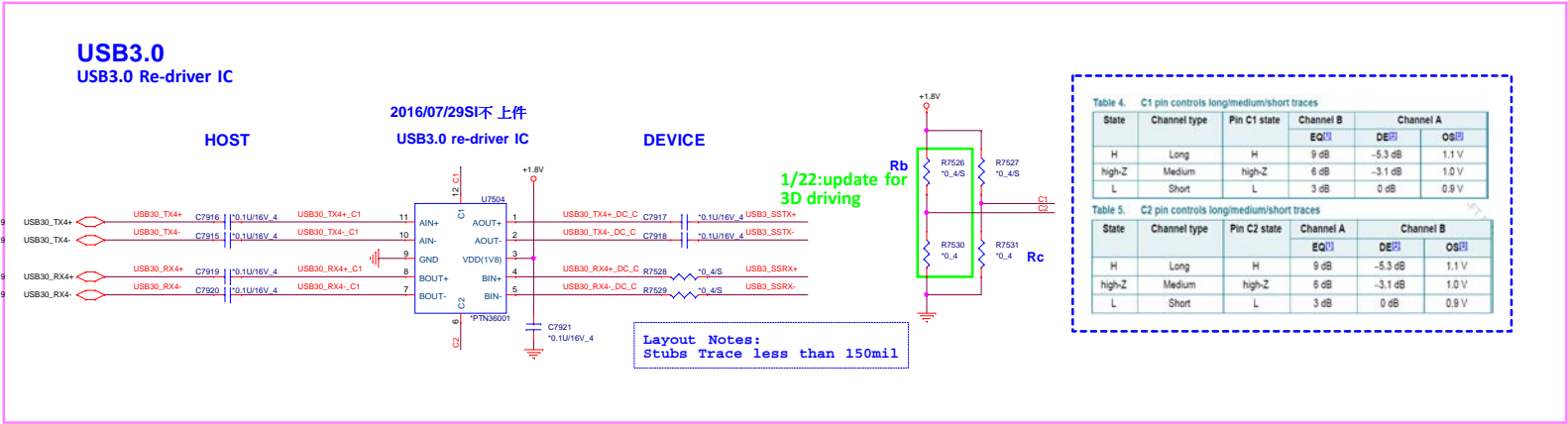
Size	Document Number	Rev
Custom	30 - USB3.0/DB	1A
Date: Thursday, November 10, 2016		Sheet 30 of 52

+5V 26,27,28,29,32,38,46,49
+3VPCU 5,10,21,30,33,37,38,40,41
+3V 5,8,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51
+1.8V 22,28,47,51

BOM: 3D CAM/HD CAM combine

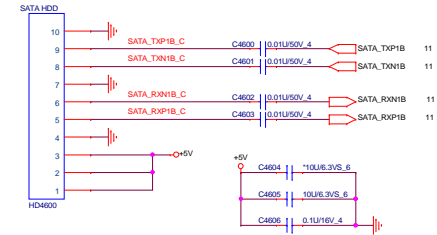


BOM: 3D CAM/HD CAM combine

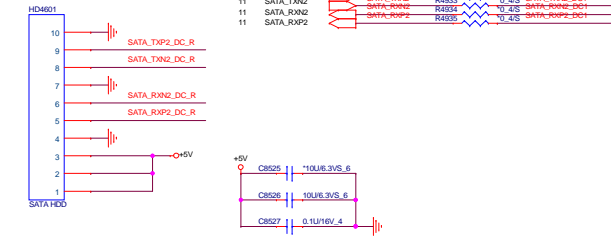


+VIN 26,38,39,40,41,42,43,44,45,46,47,48,49,50,52
+5V 26,27,28,29,30,46,49
+5V 6,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,33,34,35,36,37,38,43,46,50,51

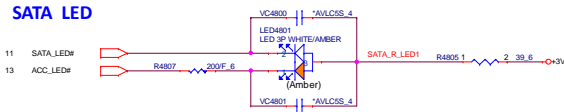
HDD



HDD (Close to ODD)



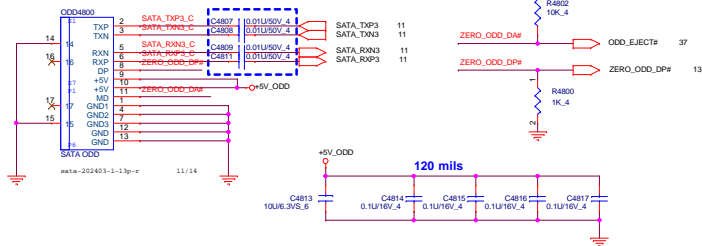
SATA LED



SATA_TXP2.DC1 C4824 0.01uF/50V_4 SATA_TXP2.DC_R
SATA_TXN2.DC1 C4825 0.01uF/50V_4 SATA_TXN2.DC_R
SATA_RXN2.DC1 C4826 0.01uF/50V_4 SATA_RXN2.DC_R
SATA_RXP2.DC1 C4827 0.01uF/50V_4 SATA_RXP2.DC_R

SATA ODD

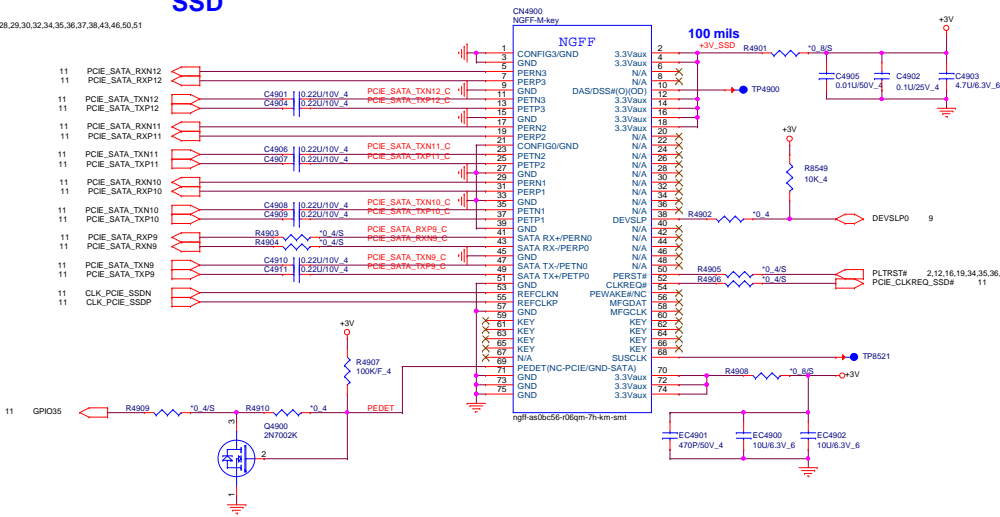
Bypass CAP close CON



ZERO_PWR_ODD:
High : ODD power down
Low : ODD power on

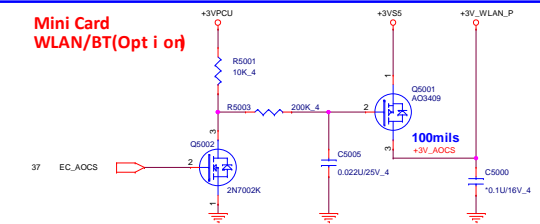
+3VPCU 5,10,21,30,37,38,40,41
+3V5S 10,12,14,16,37,41,42,46,47,48
+3V 5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,34,35,36,37,38,43,46,50,51

SSD

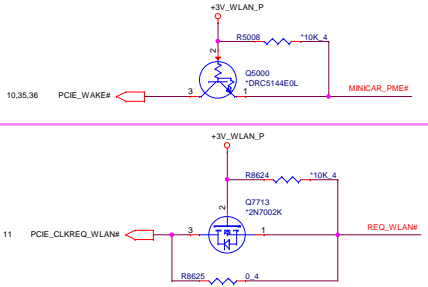


33

Mini Card
WLAN/BT(Optional)

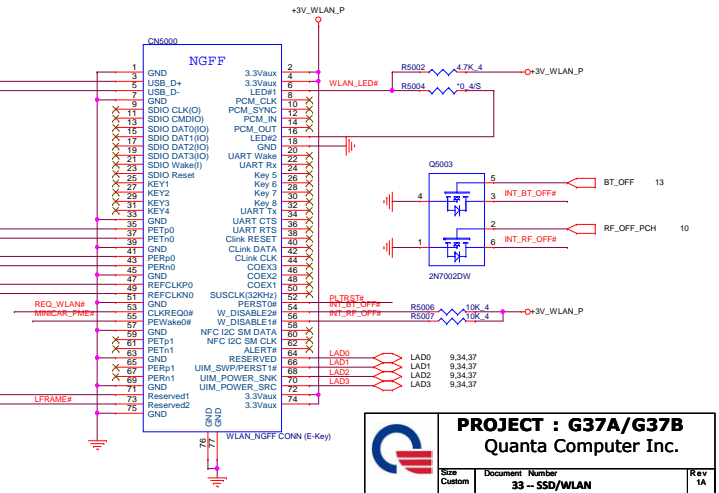
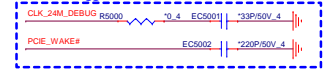



Support Wake Function or Reserve



0303 Reserved the MOSFET at CLKREQ#
even the current leakage test passed for
HP requested

For EMI Suggest i on





PROJECT : G37A/G37B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	33 - SSD/WLAN	1A
Date: Thursday, November 10, 2016	Sheet 33	of 62

PN:AL009665K01

For SWR mode support RTL8111HSH/RTL8107ESH

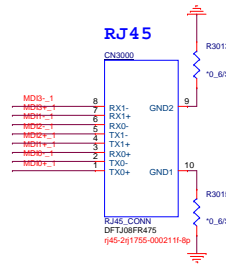
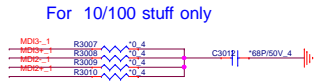
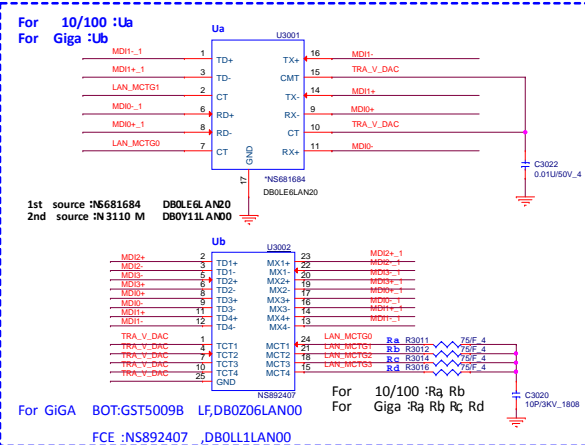
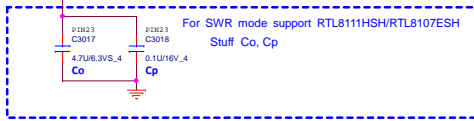
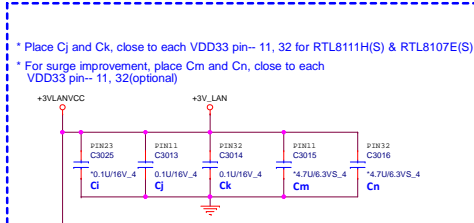
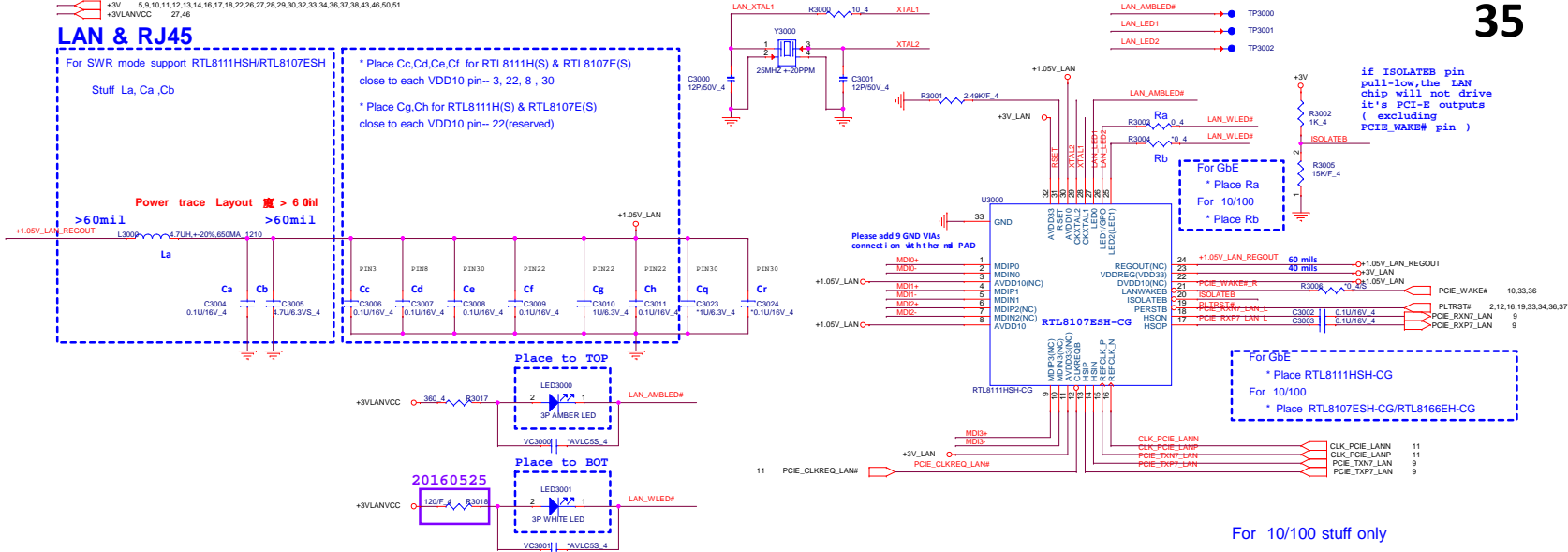
Stuff La,Ca,Cb

* Place Cc,Cd,Ce,Cf for RTL8111H(S) & RTL8107E(S)
close to each VDD10 pin-- 3, 22, 8, 30

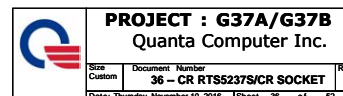
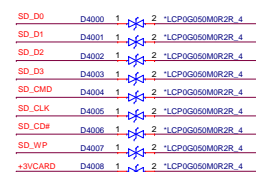
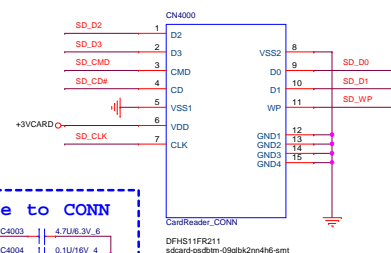
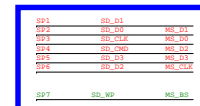
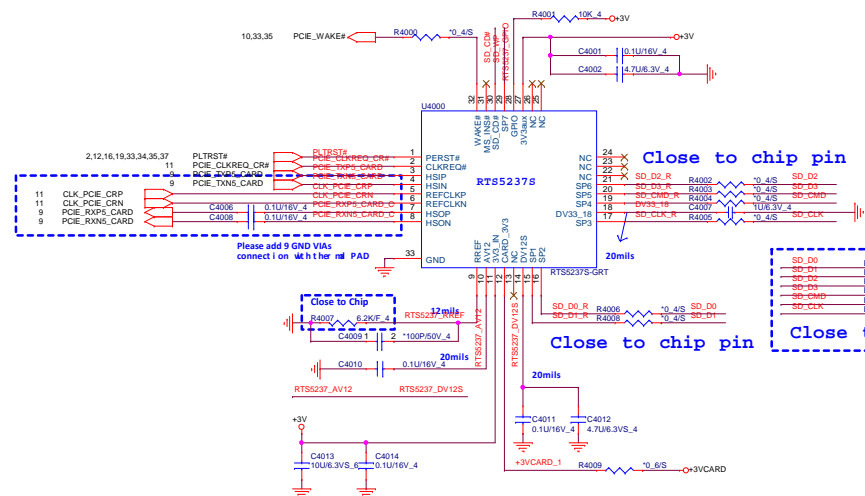
* Place Cg,Ch for RTL8111H(S) & RTL8107E(S)
close to each VDD10 pin-- 22(reserved)

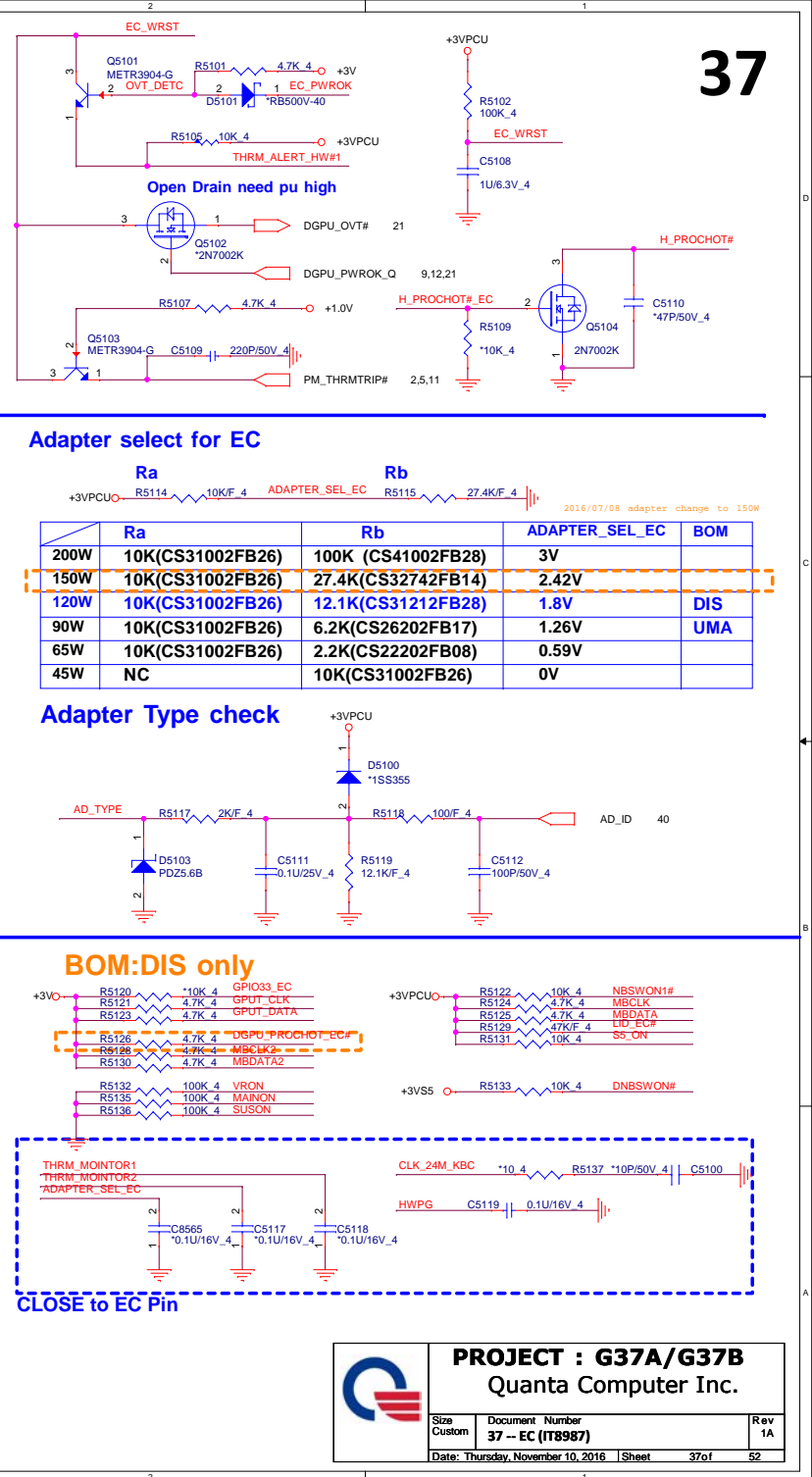
Power trace Layout 寬 > 60mil

>60mil



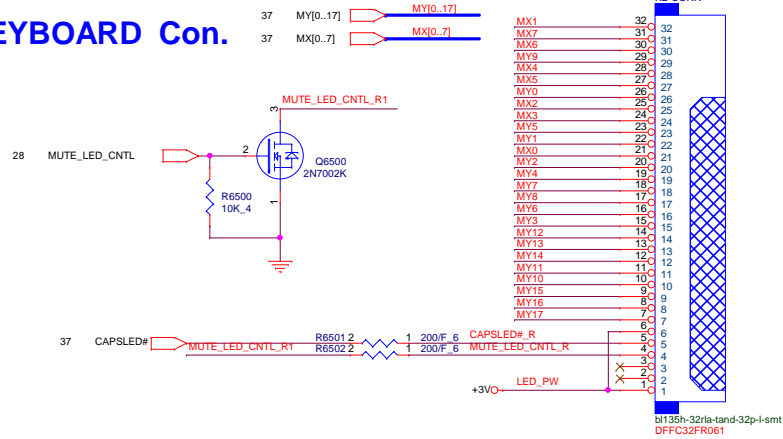
	PROJECT : G37A/G37B		
	Quanta Computer Inc.		
Size	Document Number	Rev	IA
Custom	35 - LAN RTL8107ESH-CG/RJ45		
Date: Thursday, November 10, 2016	Sheet	35	of 52



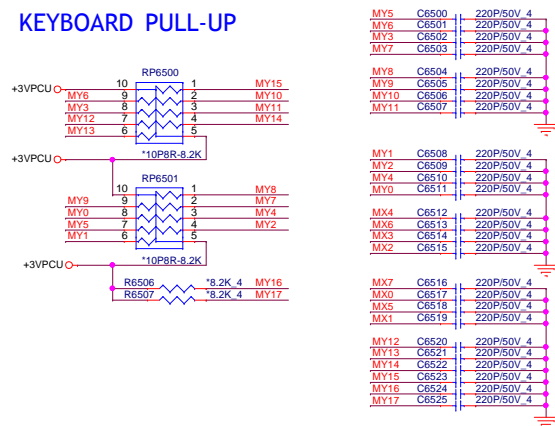


+VIN 26,32,39,40,41,42,43,44,45,46,47,48,49,50,52
 +5V 26,27,28,29,32,46,49
 +3VPCU 5,10,21,30,33,37,40,41
 +3VS5 10,12,14,16,33,37,41,42,46,47,48
 +3VSUS 46
 +3V 5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,43,46,50,51

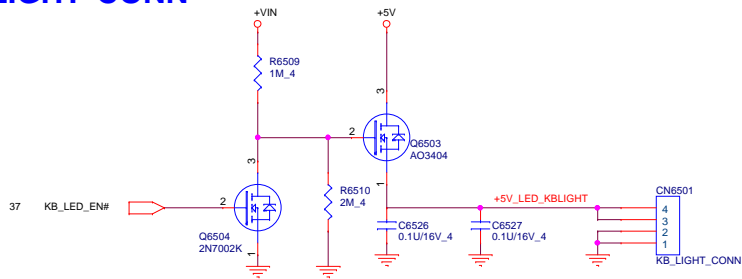
KEYBOARD Con.



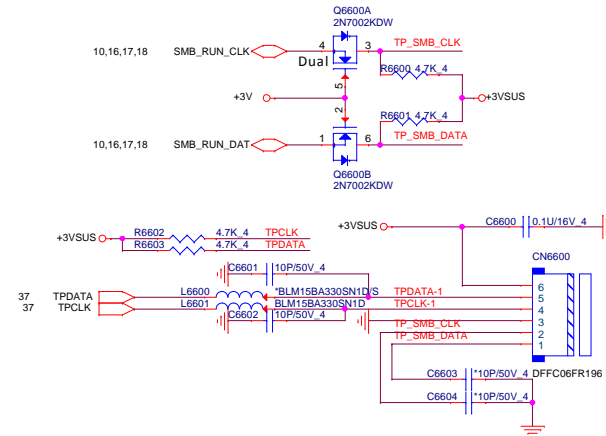
KEYBOARD PULL-UP



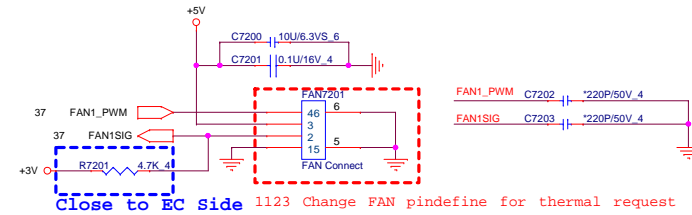
KB LIGHT CONN



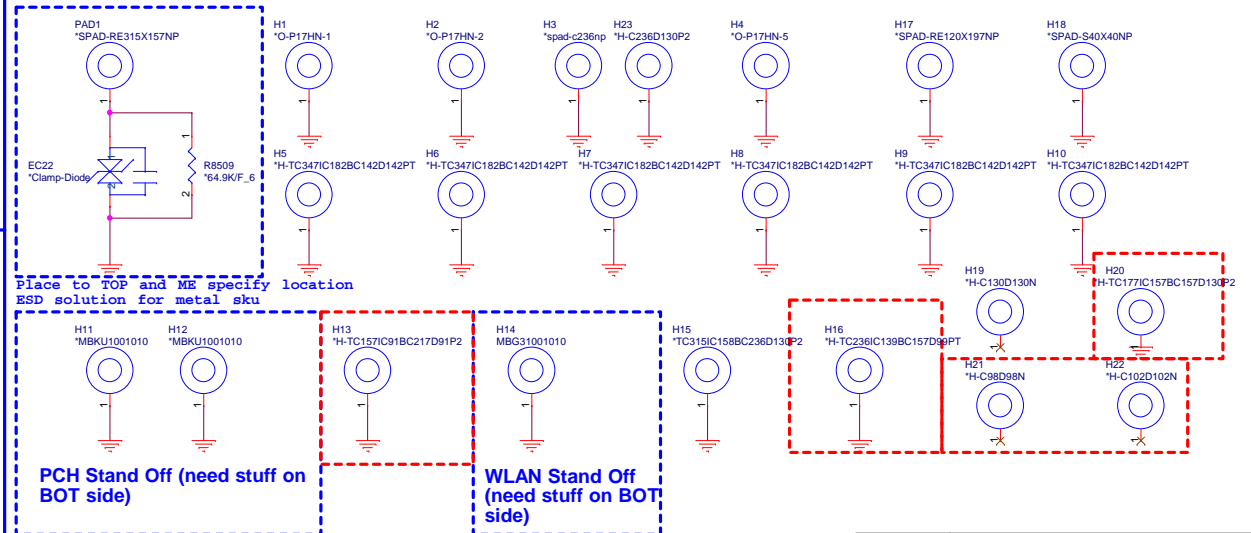
Touch Pad Connector

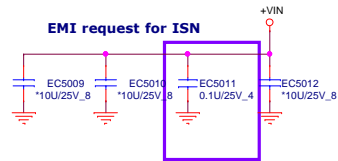
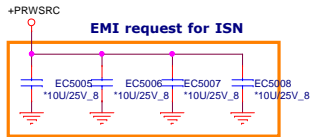


FAN



HOLE



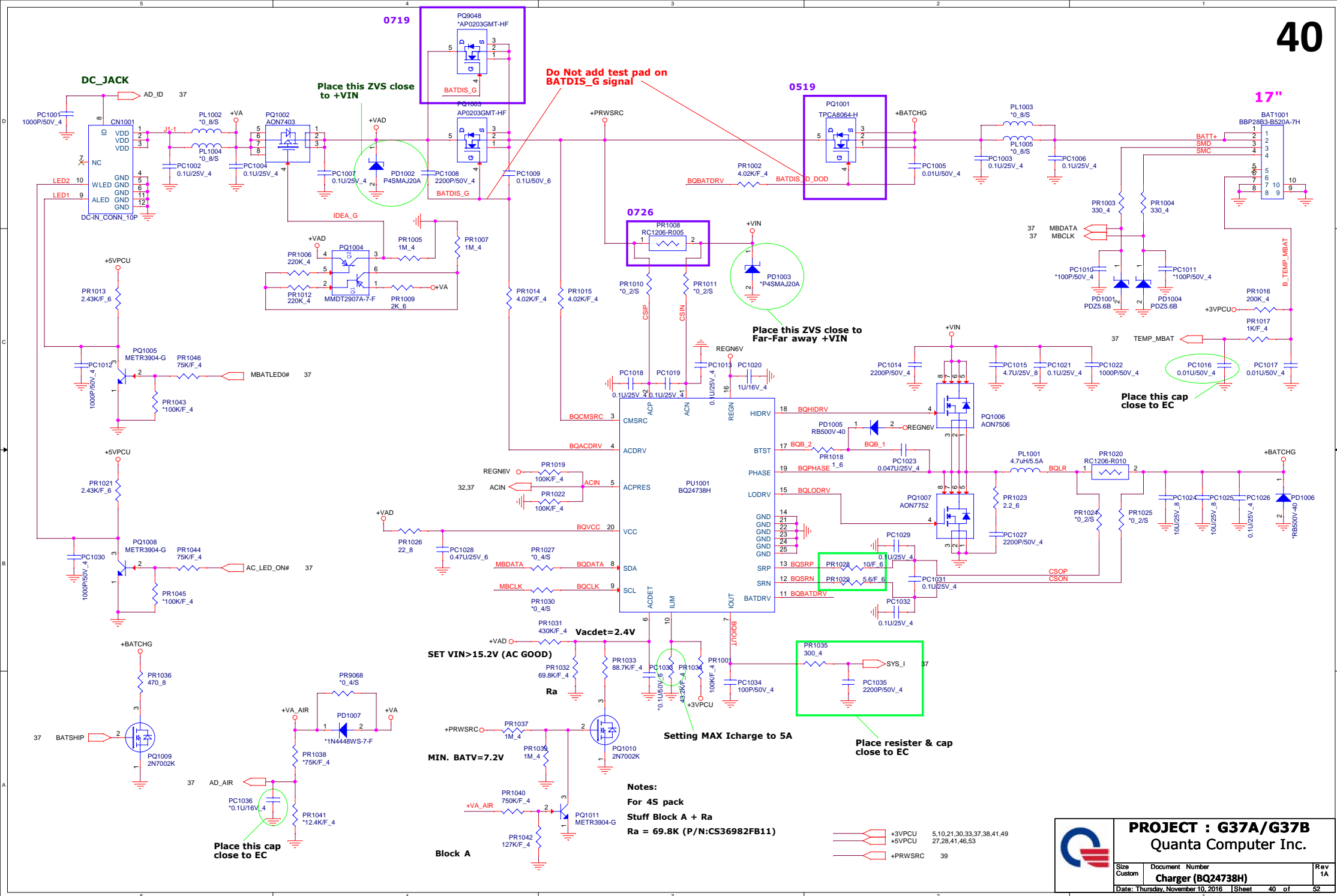


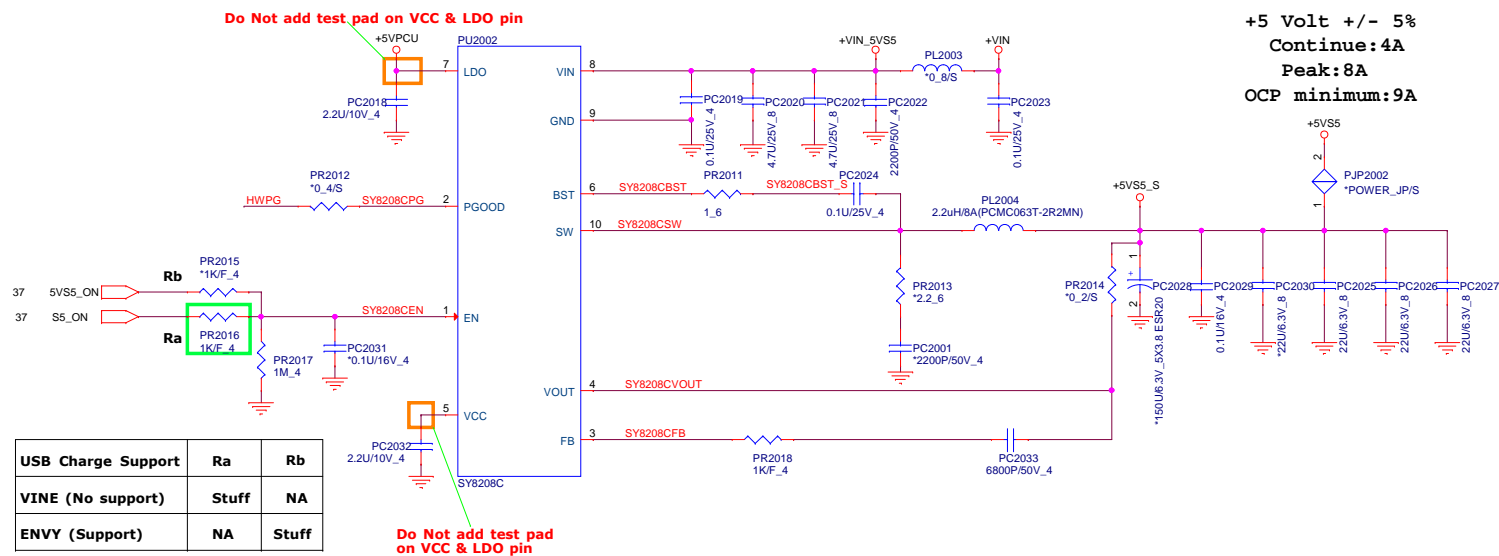
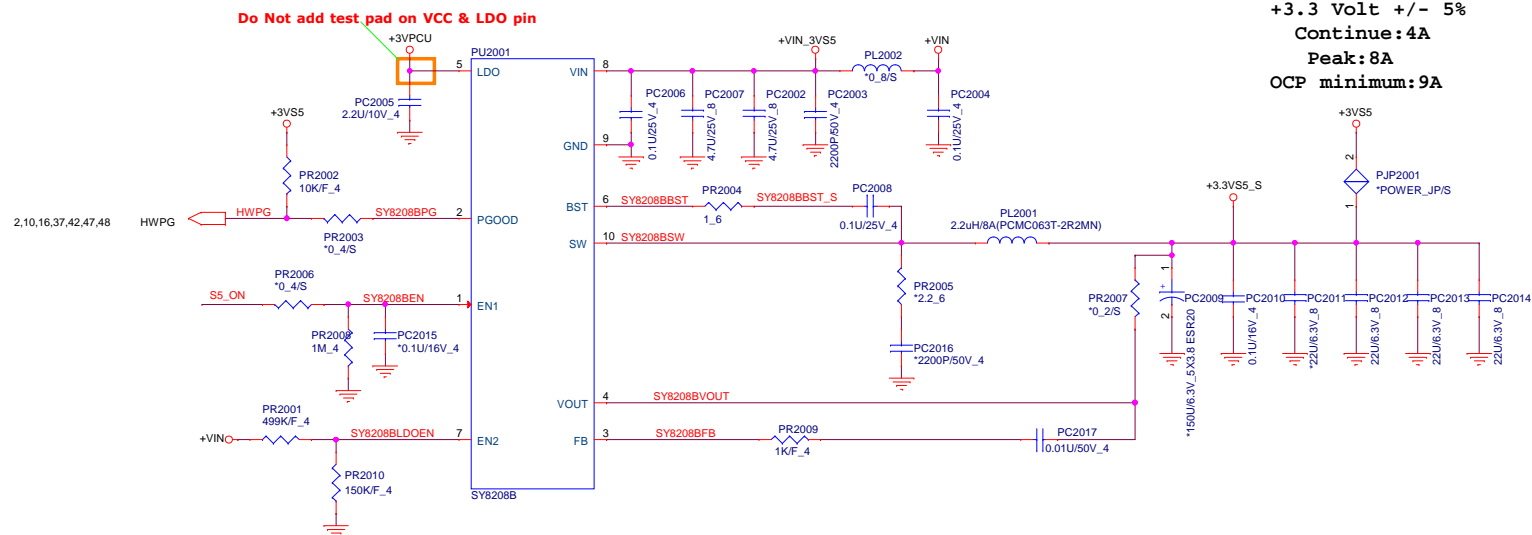
20160308 MV change for EMI request



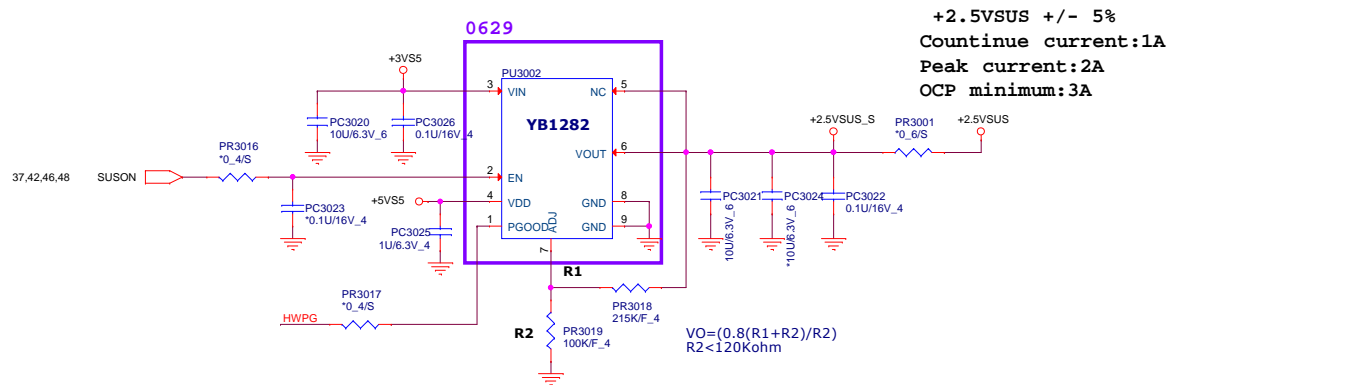
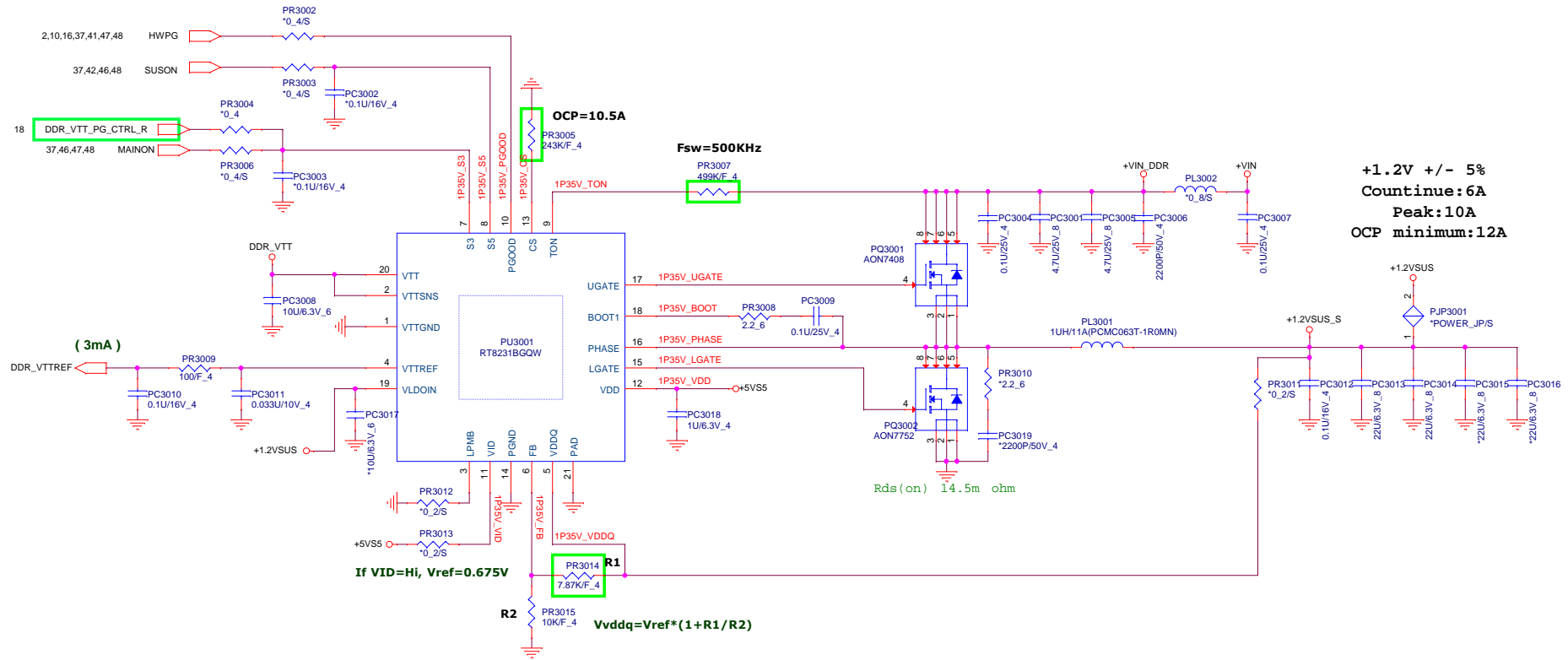
PROJECT : G37A/G37B
Quanta Computer Inc.

Size Custom	Document Number RF Solution	Rev 1A
Date: Thursday, November 10, 2016		Sheet 39 of 52

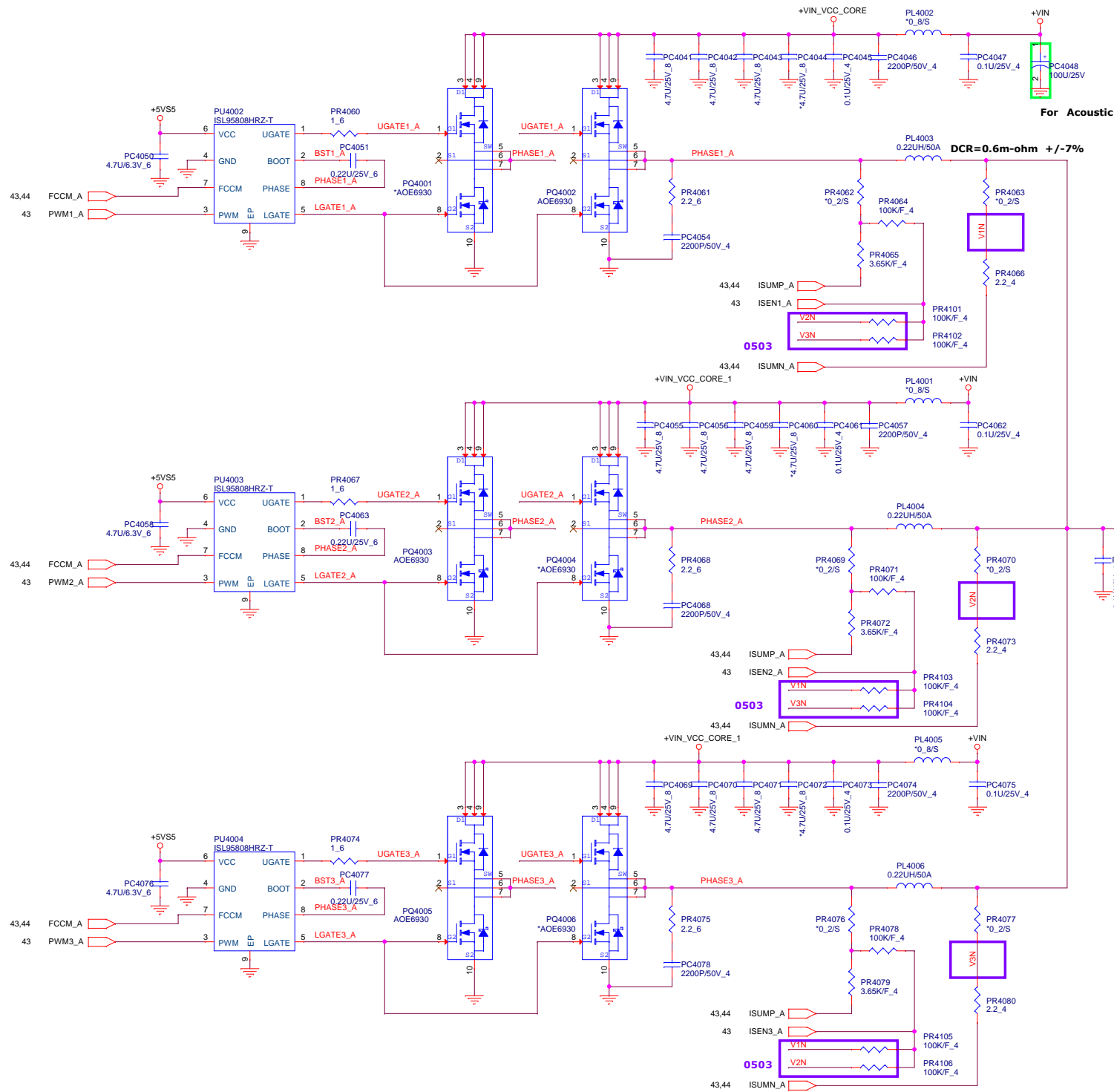




+VIN 26,32,38,39,40,42,43,44,45,46,47,48,49,52
 +3VS5 10,12,14,16,26,33,37,42,46,47,48
 +5VS5 10,28,29,30,42,43,44,45,46,47,48,49,50,51,52,53
 +3VPCU 5,10,21,30,33,37,38,40,49
 +5VPCU 27,28,40,46,53

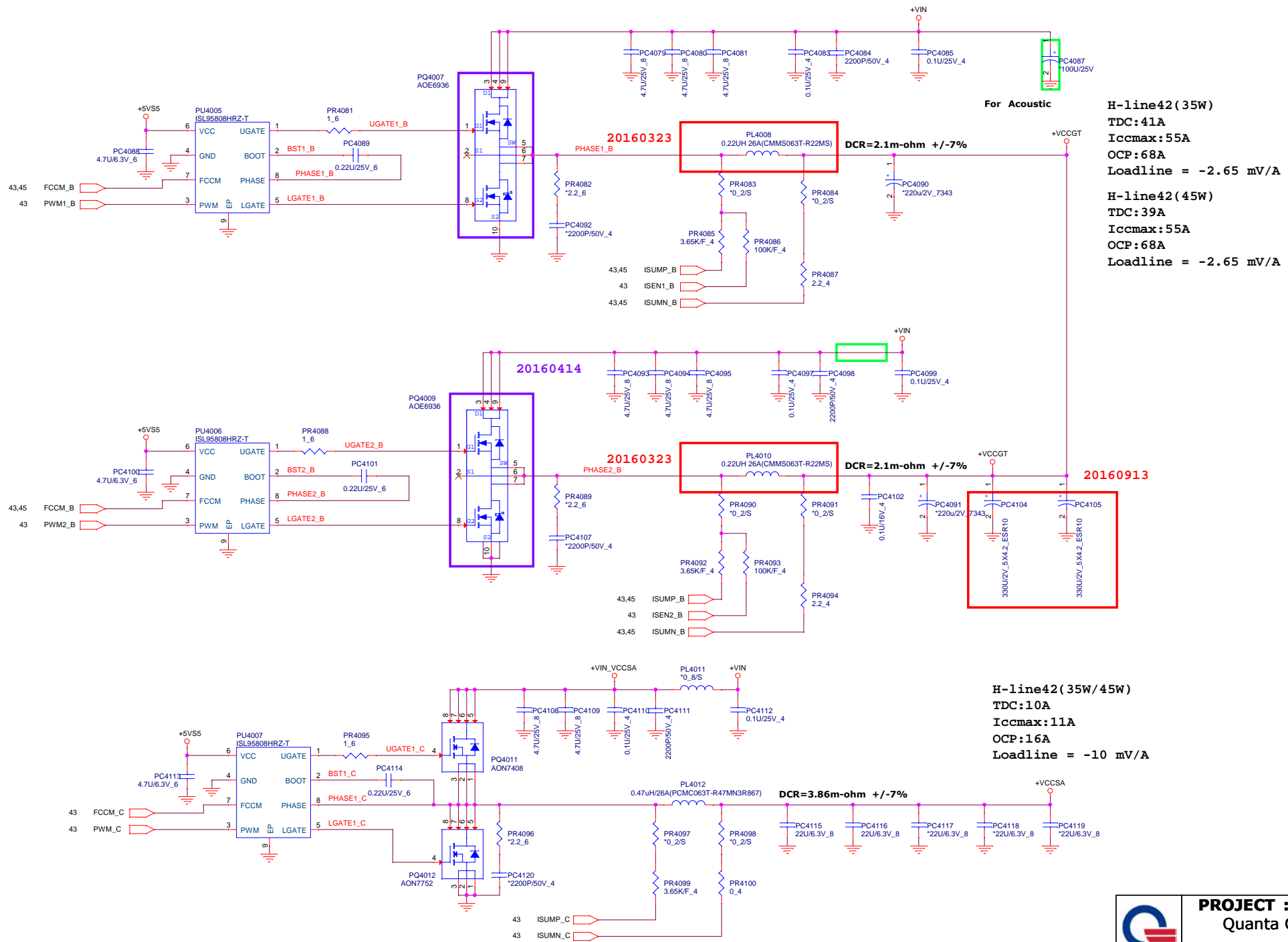


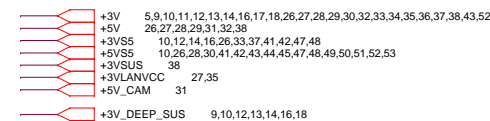
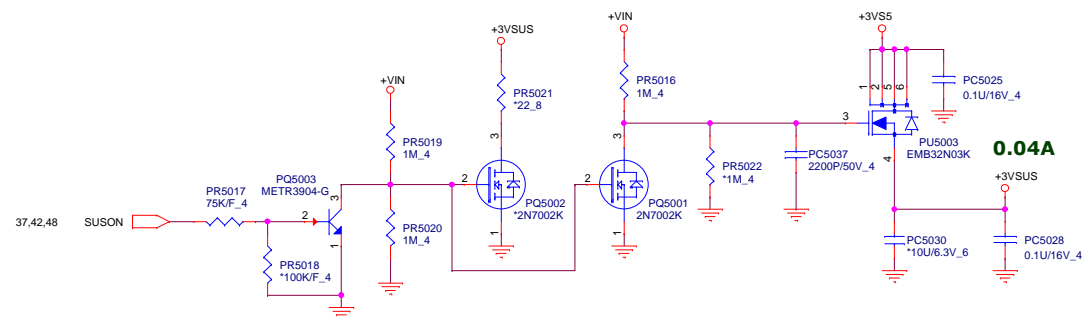
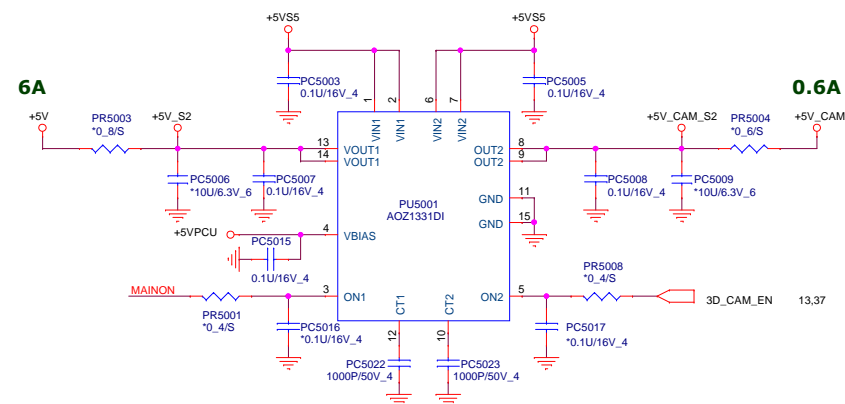
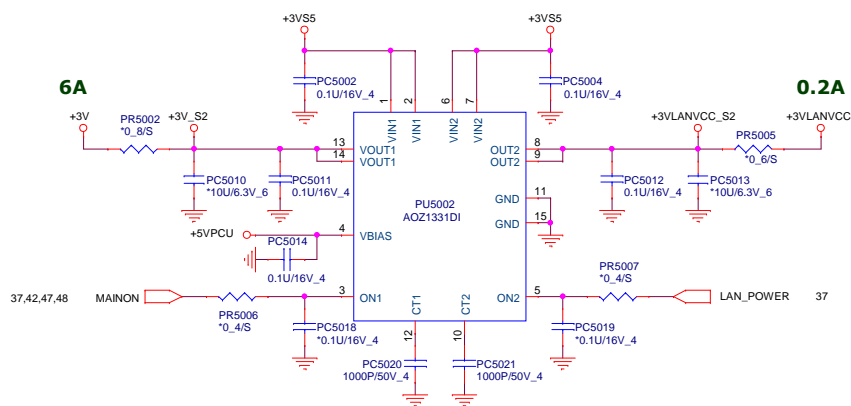
+VIN	26,32,38,39,40,41,43,44,45,46,47,48,49,52
+5VS5	10,26,28,30,41,43,44,45,46,47,48,49,50,51,52,53
+1.2VSUS	2,6,10,17,18,48,53
DDR_VTT	17,18
+2.5VSUS	17,18



PROJECT : G37A/G37B
Quanta Computer Inc.

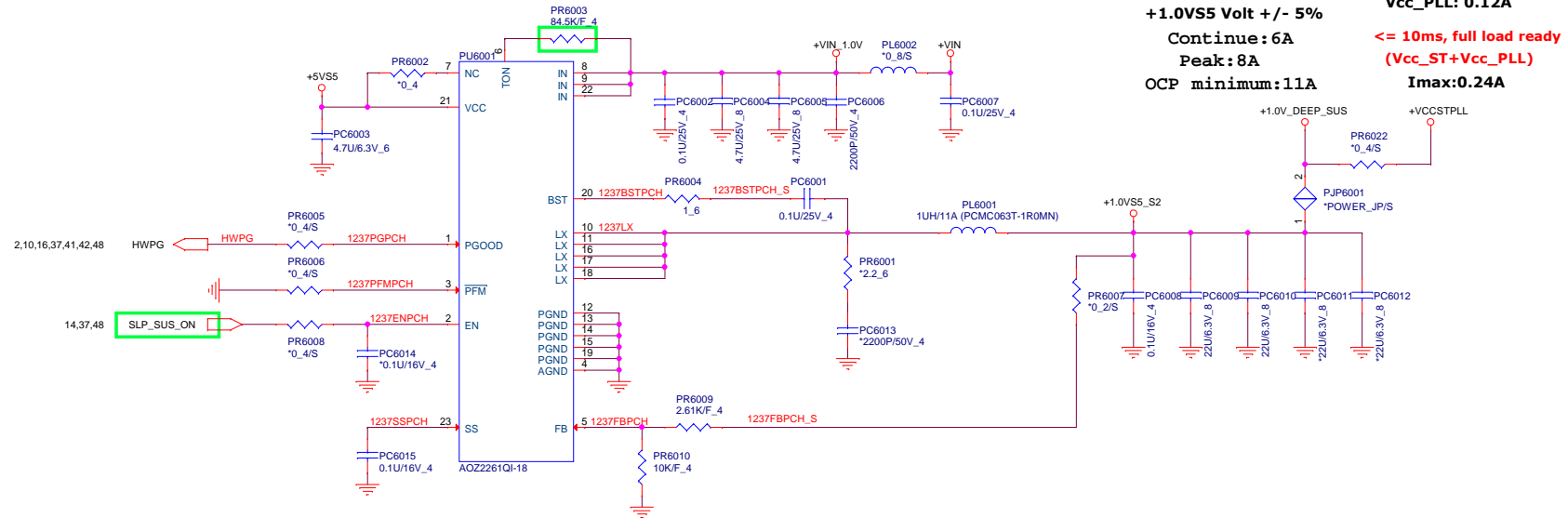
Size Custom	Document Number +VCC_CORE (ISL95808HRZ-T)	Rev 1A
Date:	Thursday, November 10, 2016	Sheet 44 of 52





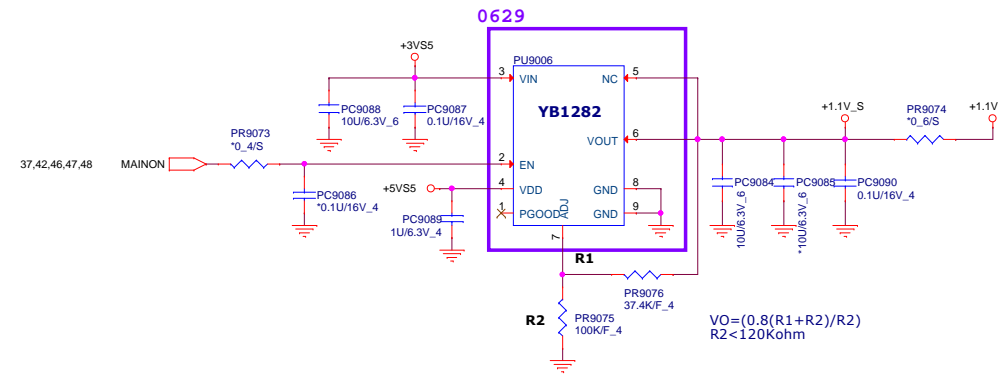
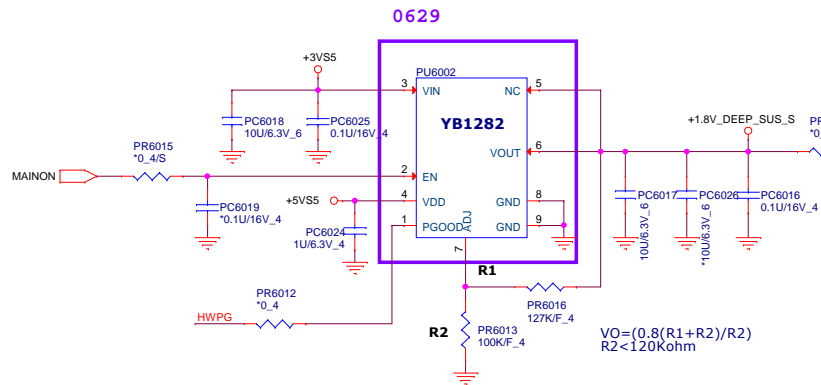
PROJECT : G37A/G37B
Quanta Computer Inc.

Size Custom	Document Number Load switch IC (AOZ1331D)	Rev 1A
Date: Thursday, November 10, 2016		Sheet 46 of 52



+1.1V +/- 5%
TDC: 1A
EDP: 2A

+1.8V +/- 5%
TDC: 1A
EDP: 2A



+VIN 26,32,38,39,40,41,42,43,44,45,46,48,49,52
+3VS5 10,12,14,16,26,33,37,41,42,46,48
+5VS5 10,26,28,30,41,42,43,44,45,46,48,49,50,51,52,53
+1.0V_DEEP_SUS 10,11,14,16,48
+1.8V 28,31,53
+VCCSTPLL 2,6,43

Volume Segment

Vcc_STG: 0.04A

Vcc_IO: 5.5A

<= 10ms full load ready

Imax:5.5A

Imax:0.04A

<= 240us, full load ready

TDC:0.26A

Reserve for separating +1.0V and VCCIO

+0.95 +/- 5%
Continue: 4A
Peak: 5.5A
OCP minimum: 8A

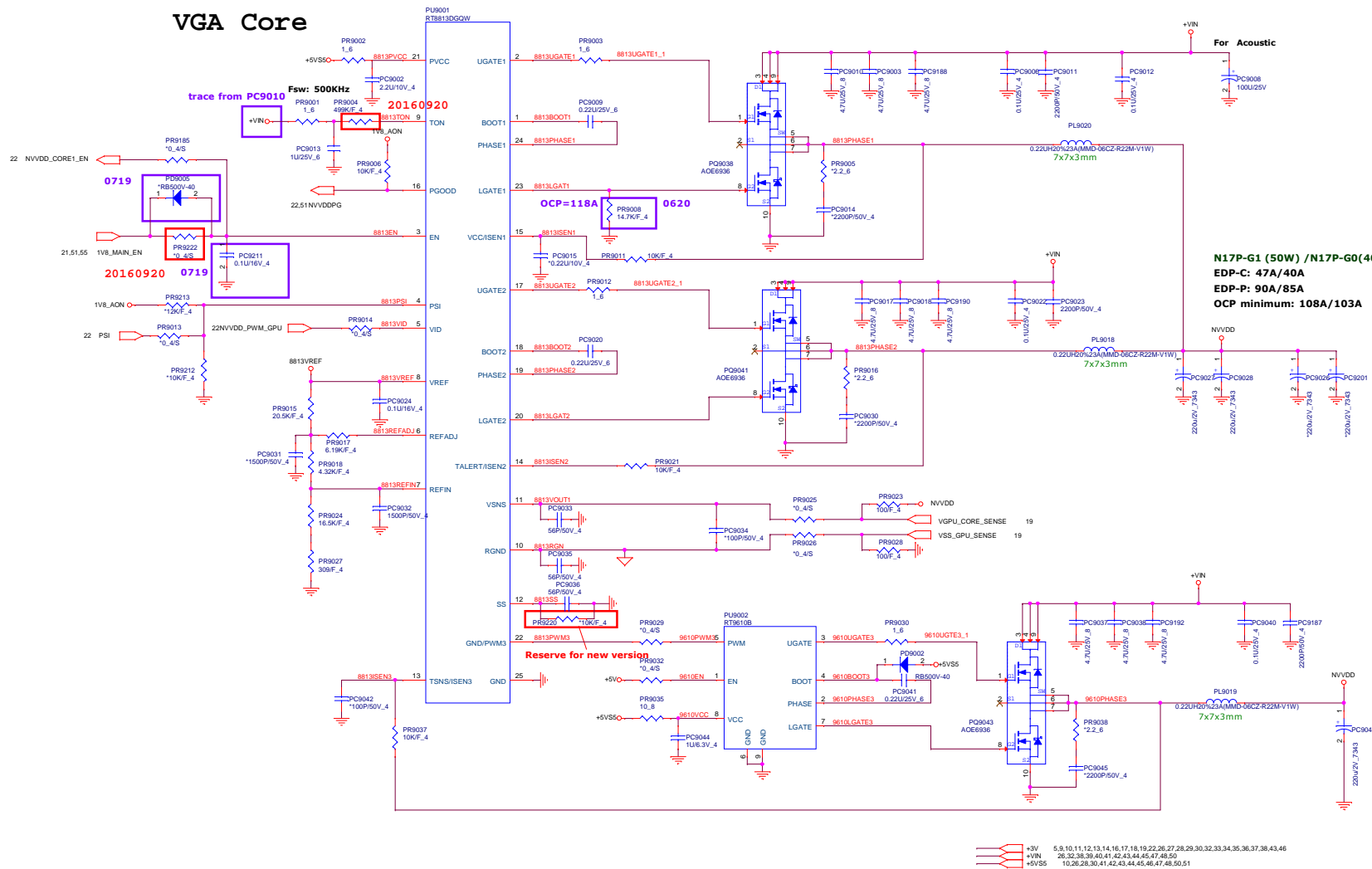
+1.0V	2,5,6,10,16,37
+3VS5	10,12,14,16,26,33,37,41,42,46,47
+5VS5	10,26,28,30,41,42,43,44,45,46,47,48,50,51,52,53
+VCCIO	3,6,16
+1.0V_DEEP_SUS	10,11,14,16,47
+1.2V_VCCPLL_OC	6
+1.2VSUS	2,6,10,17,18,42,53



PROJECT : G37A/G37B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL+VCCIO	1A
Date: Thursday, November 10, 2016	Sheet 48 of 52	

VGA Core



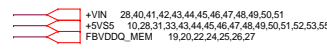
NVDDS

- Ripple Current:**
Irip=7.79A
- Ripple Voltage:**
ESR/1=9mohm
Vrip=70.11mV
- MOSFET Spec:**
L-side MOSFET: FDP5030
Rds(ON)=3mohm (Vgs=4.5 V)
I cont = 25A (T = 25 °C)
I pulse=503A
- Frequency:**
F=500KHz (PR224=300k ohm)
- OCp:**
Set = PR9008 to 14.7K
Vtrip= PR9008*10uA-40mV=107V
Iocp=(Vtrip/Rdsn) + Irip/2
= 39.565A (1 phase)
Total OCp=39.565*3=118.7A (3 phase)



PROJECT : G37A/G37B
Quanta Computer Inc.

Doc Name	Doc Number	Rev
Custom	+VGACORE (RT8813C)	1A
Date:	Thursday, November 10, 2011	Sheet 49 of 52



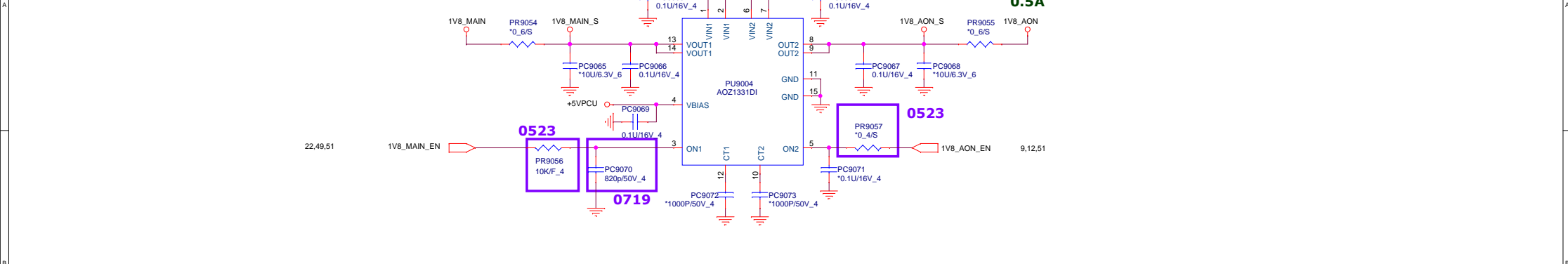
1. Ripple Current:
 $I_{rip}=5.34A$ $V_o=1.35V$
 $I_{rip}=5.88A$ $V_o=1.5V$

2. Ripple Voltage:
 $ESR/1=9mohm$
 $V_{rip}=48.06mV$ $V_o=1.35$
 $V_{rip}=53mV$ $V_o=1.5$

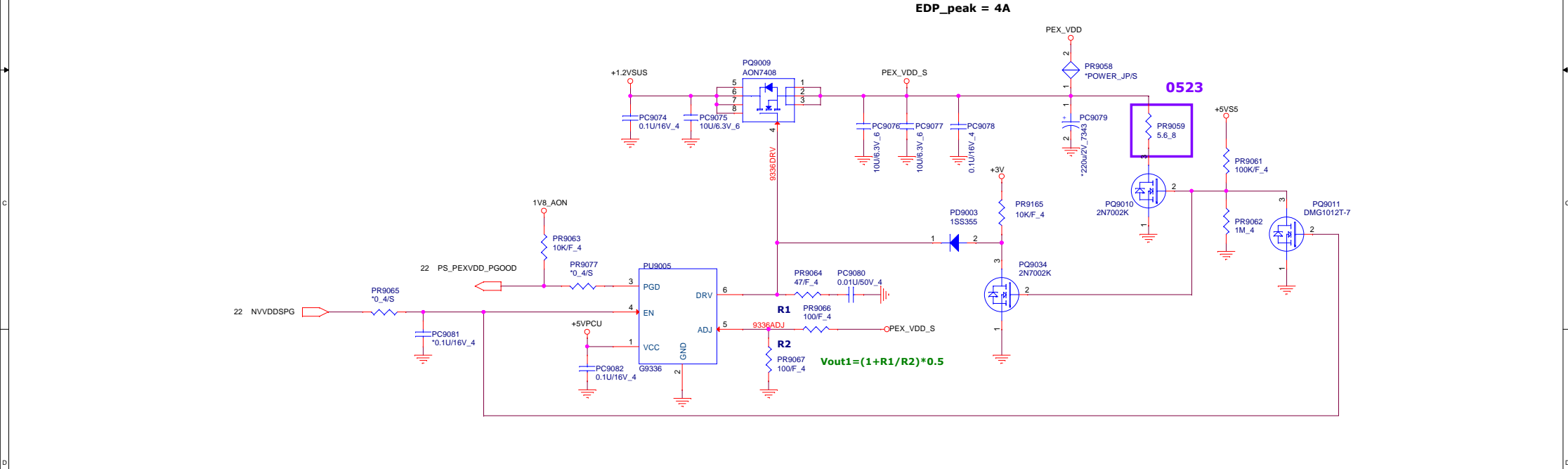
3.MOSFET Spec:
 L-side MOSFET: FDMOS3669S
 $R_{ds}(ON)=5.2mohm$ ($V_{gs}=4.5V$)
 $I_{cont} = 18A$ ($T=25^{\circ}C$)
 $I_{pulse}=60A$

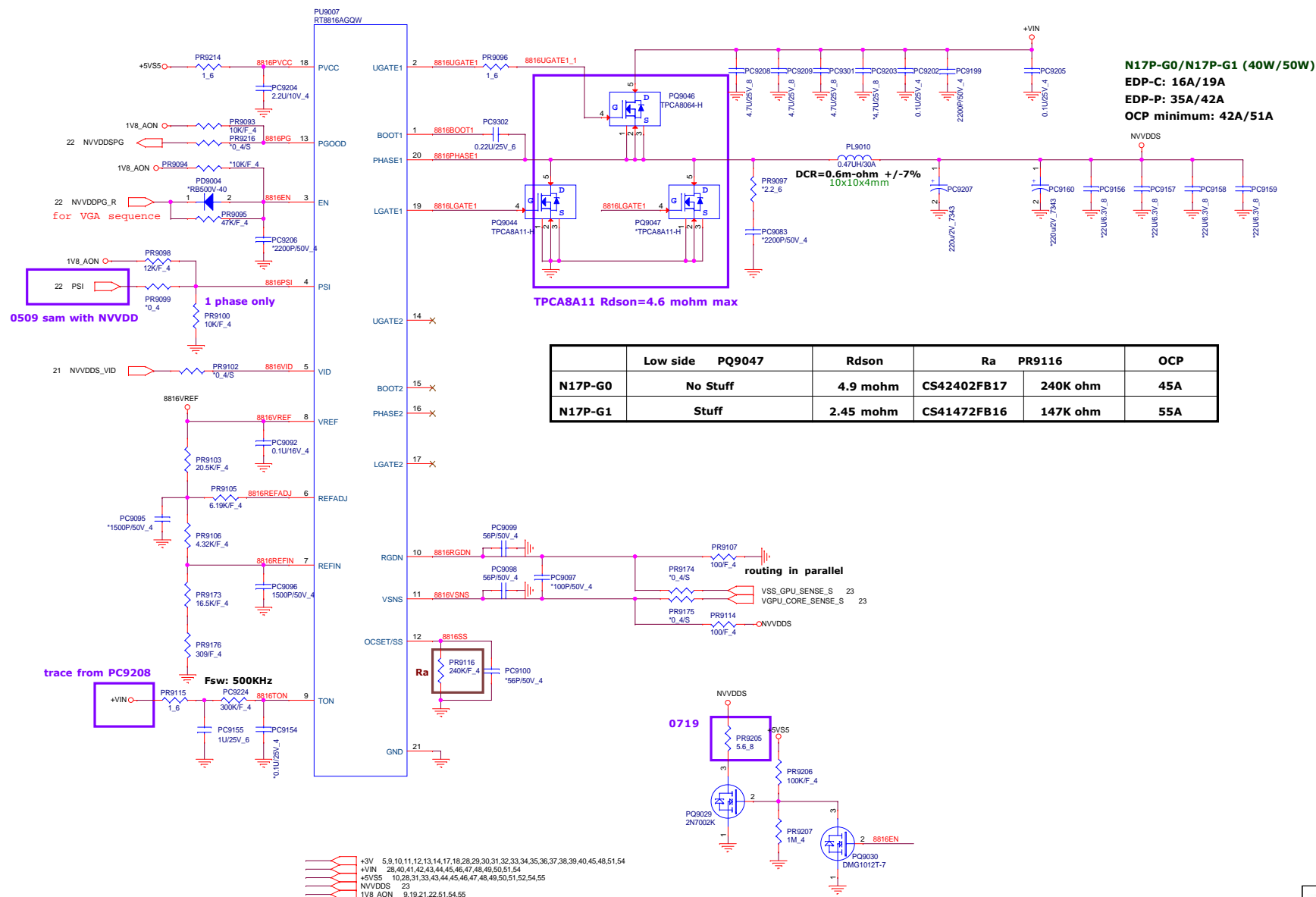
4. Frequency:
 $F=500KHz$ ($PR9145=300k\ ohm$)

5. OCC:
 $Set = PR9147$ to $133K$ $V_o=1.35$
 $V_{trip}=PR9147*10uA/12=110.83mV$
 $locp=(V_{trip}/R_{ds(on)}) + I_{ripple}/2 = 24A$



B	<p>+1.0V_GFX Volt +/- 5%</p> <p>EDP=3A</p> <p>EDP_peak = 4A</p>	E
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1. **Ripple Current:**
Irip=3.65A
2. **Ripple Voltage:**
ESR/1=9mohm
Vrip=32.85mV
3. **Inductor Spec:**
Isat=40A
Idc=30A
DCR=1.68mohm
4. **MOSFET Spec:**
L-side MOSFET: TPCA8A11-H
Rds(ON)=4.6mohm (Vgs=4.5 V)
I cont = 28A (T = 25 °C)
I pulse=140A
5. **Frequency:**
F=500KHz (PR9224=300k ohm)
6. **OCP:**
Set = PR9116 to 240K
Vtrip= PR9116*10uA/12=200mV
Iocp=(Vtrip/Rds(on)) + Iripple/2 = 45A

Set = PR9116 to 147K
Vtrip= PR9116*10uA/12=122.5mV
Iocp=(Vtrip/Rds(on)) + Iripple/2 = 55A